US009270502B2

(12) **United States Patent**
Eo et al.

(10) **Patent No.: US 9,270,502 B2**
(45) **Date of Patent: Feb. 23, 2016**

(54) **DIGITAL RF RECEIVER**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 180 days.

(21) Appl. No.: **13/960,555**

(22) Filed: **Aug. 6, 2013**

(65) **Prior Publication Data**

US 2014/0044221 A1 Feb. 13, 2014

(30) **Foreign Application Priority Data**

Aug. 8, 2012 (KR) 10-2012-0086998
Jun. 12, 2013 (KR) 10-2013-0067367

(51) **Int. Cl.**
H04L 25/06 (2006.01)
H04B 1/00 (2006.01)
H04L 27/38 (2006.01)

(52) **U.S. Cl.**
CPC ***H04L 25/061*** (2013.01); ***H04B 1/0007*** (2013.01); ***H04L 27/3863*** (2013.01)

(58) **Field of Classification Search**
CPC H04B 1/0003; H04B 1/001; H04B 1/0025; H04B 1/0032; H04B 1/0039; H04B 1/0021; H04B 1/005; H04B 1/006; H04B 1/0075; H03M 1/12; H03M 3/392; H04L 25/061; H04L 27/2647; H04L 27/3863
USPC 375/316, 219, 349, 350, 225, 319; 455/266, 311, 102; 708/270; 341/177
See application file for complete search history.

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(74) *Attorney, Agent, or Firm* — Kile Park Reed & Houtteman PLLC

(57) **ABSTRACT**

Embodiments provide a digital RF receiver including a signal converting unit which converts an RF signal received from an external device into a digital signal, a plurality of functional modules which processes the digital signal in accordance with a predetermined algorithm when the digital signal is input, and a signal processing controller which selects at least one of the plurality of functional modules to control the digital signal to be processed in consideration of whether an IF signal component is included in the digital signal or a sampling rate related with sampling information of the digital signal.

14 Claims, 23 Drawing Sheets

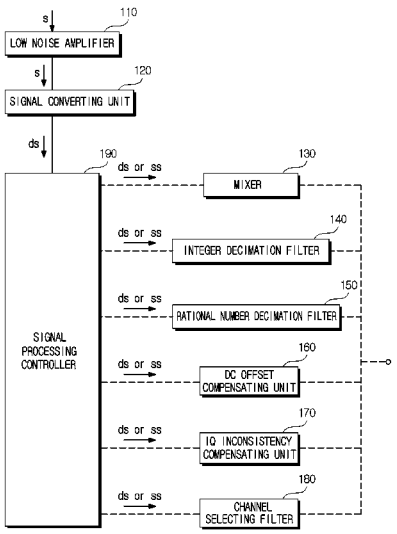


FIG.1

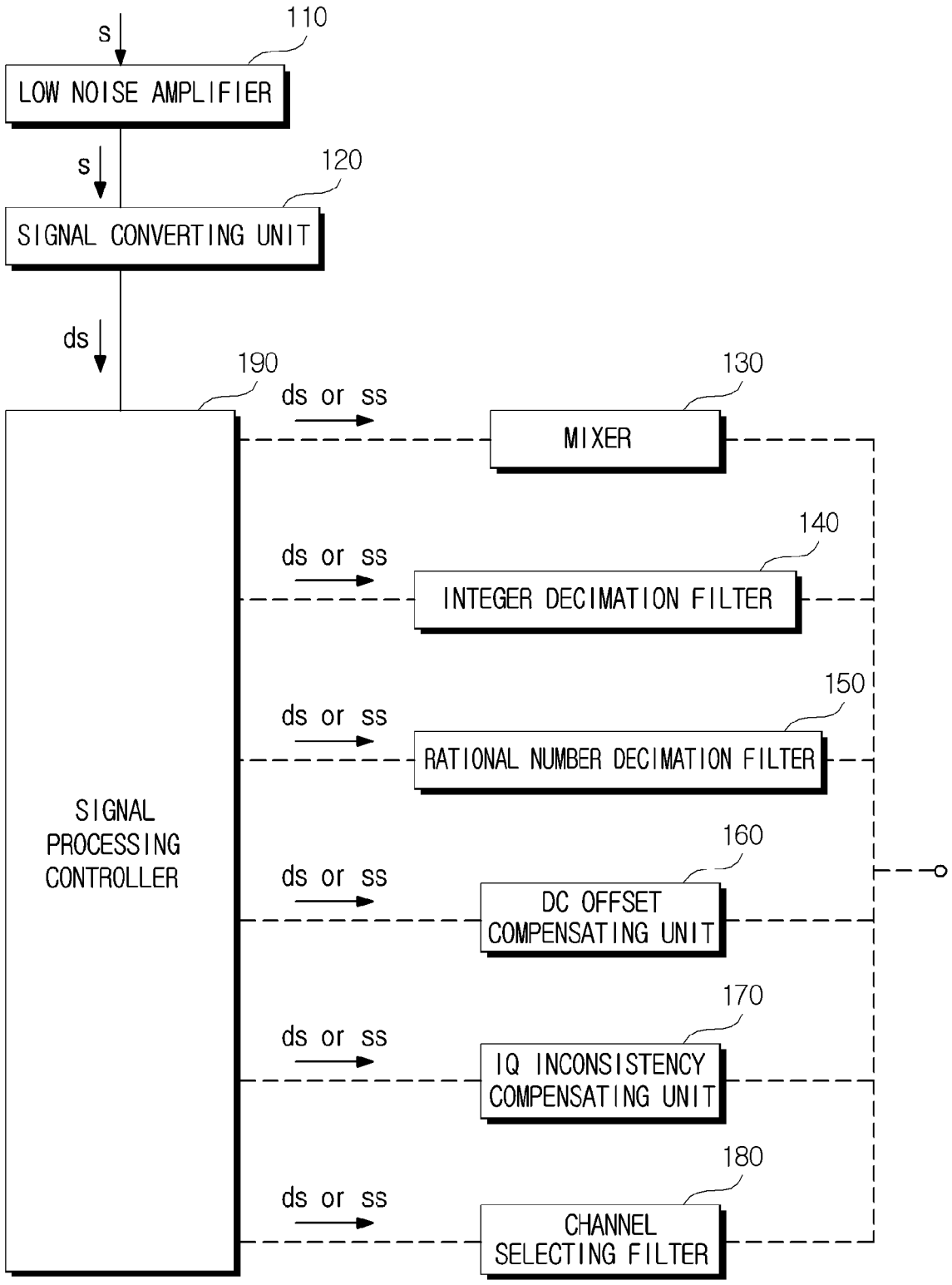

s
110
LOW NOISE AMPLIFIER
s
120
SIGNAL CONVERTING UNIT
ds
190
ds or ss
130
MIXER
140
ds or ss
INTEGER DECIMATION FILTER
150
ds or ss
RATIONAL NUMBER DECIMATION FILTER
SIGNAL PROCESSING CONTROLLER
160
ds or ss
DC OFFSET COMPENSATING UNIT
170
ds or ss
IQ INCONSISTENCY COMPENSATING UNIT
180
ds or ss
CHANNEL SELECTING FILTER

FIG.2A

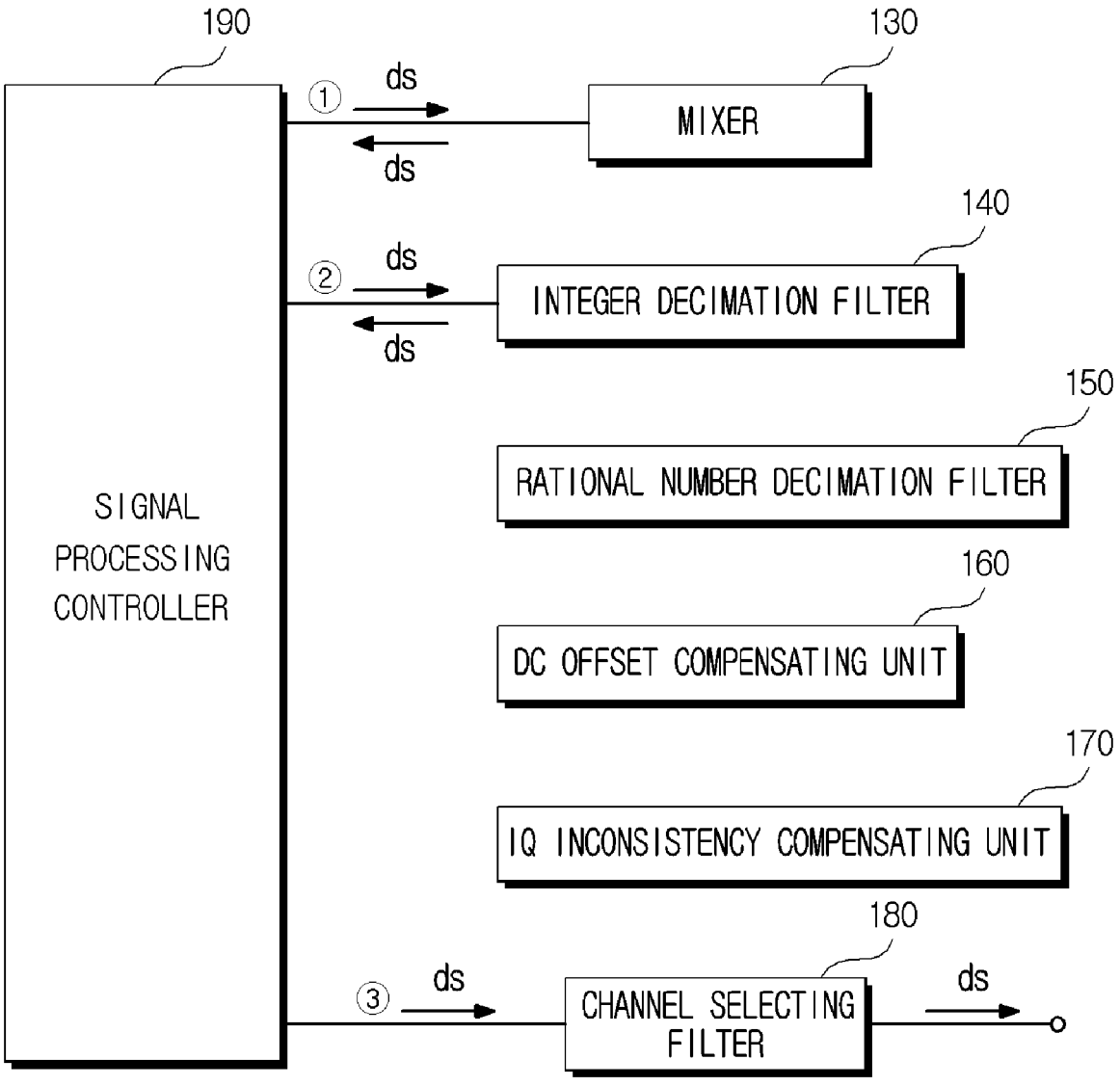
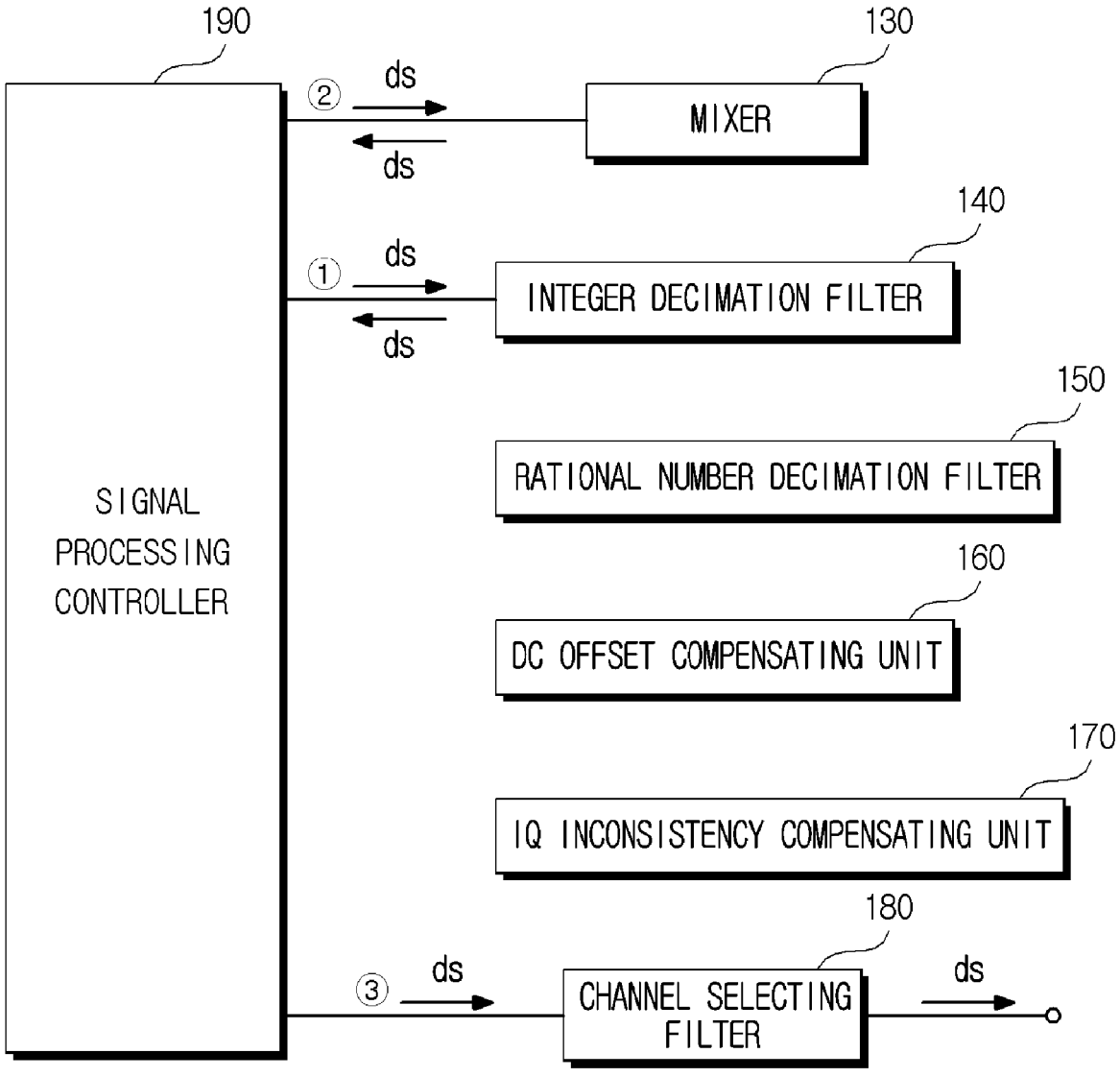

190
130
ds
①
ds
MIXER
140
ds
②
INTEGER DECIMATION FILTER
ds
150
RATIONAL NUMBER DECIMATION FILTER
SIGNAL
PROCESSING
CONTROLLER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
③
ds
CHANNEL SELECTING
FILTER
ds

FIG.2B


190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
ds
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③

FIG.3A

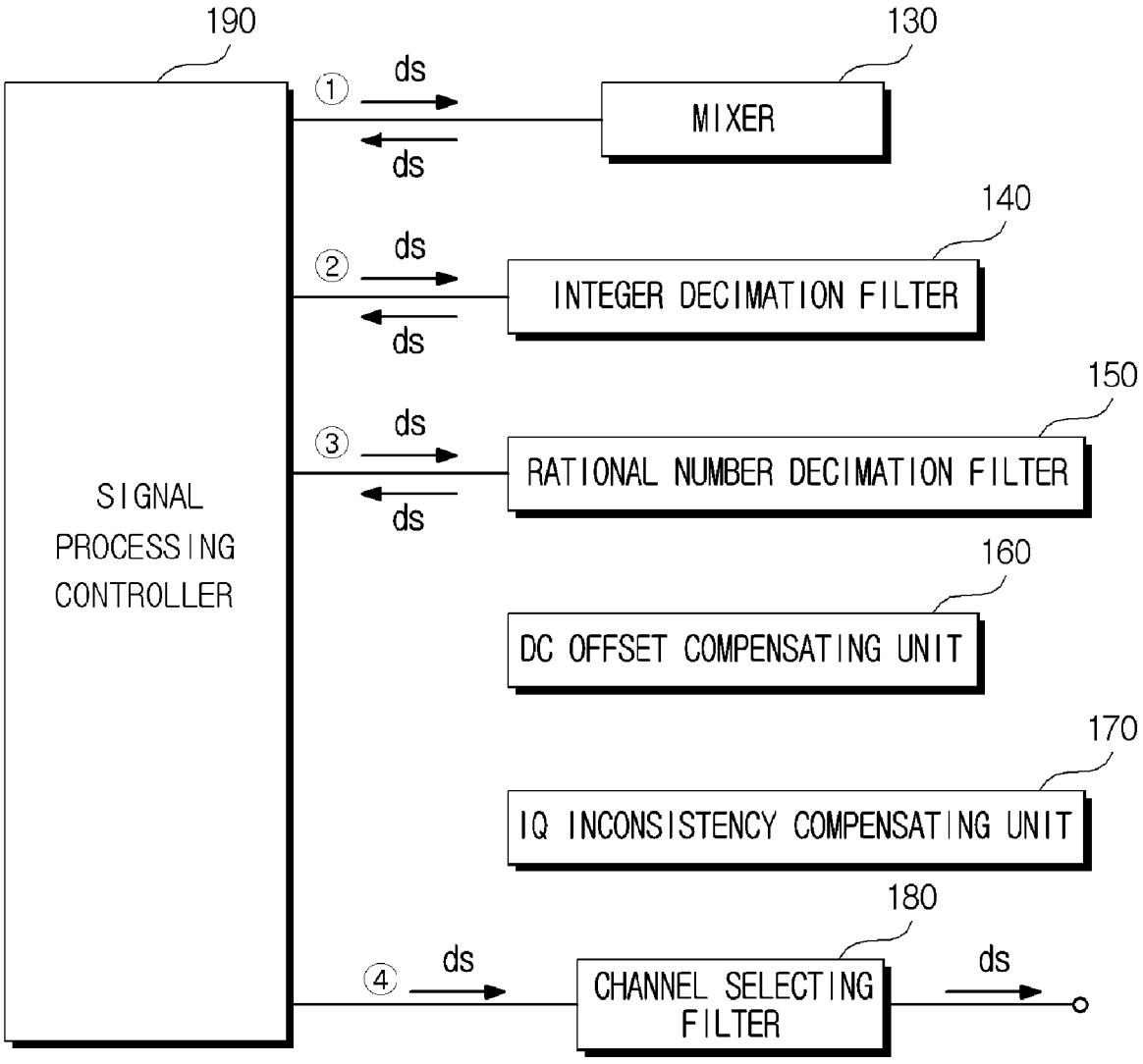
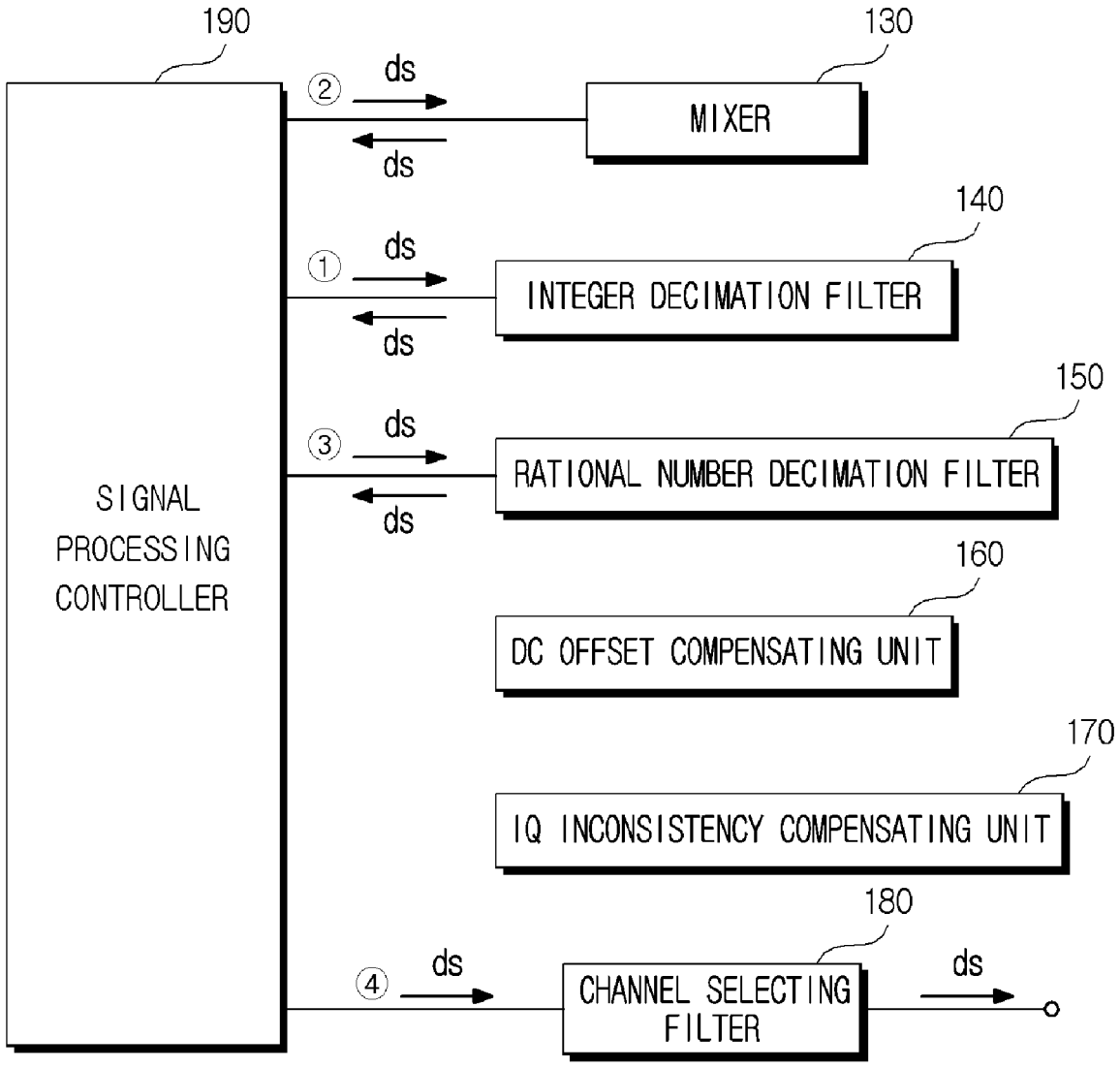

190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
① ds ds
② ds ds
③ ds ds
④ ds ds

FIG.3B


190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
ds
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②
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FIG.4A

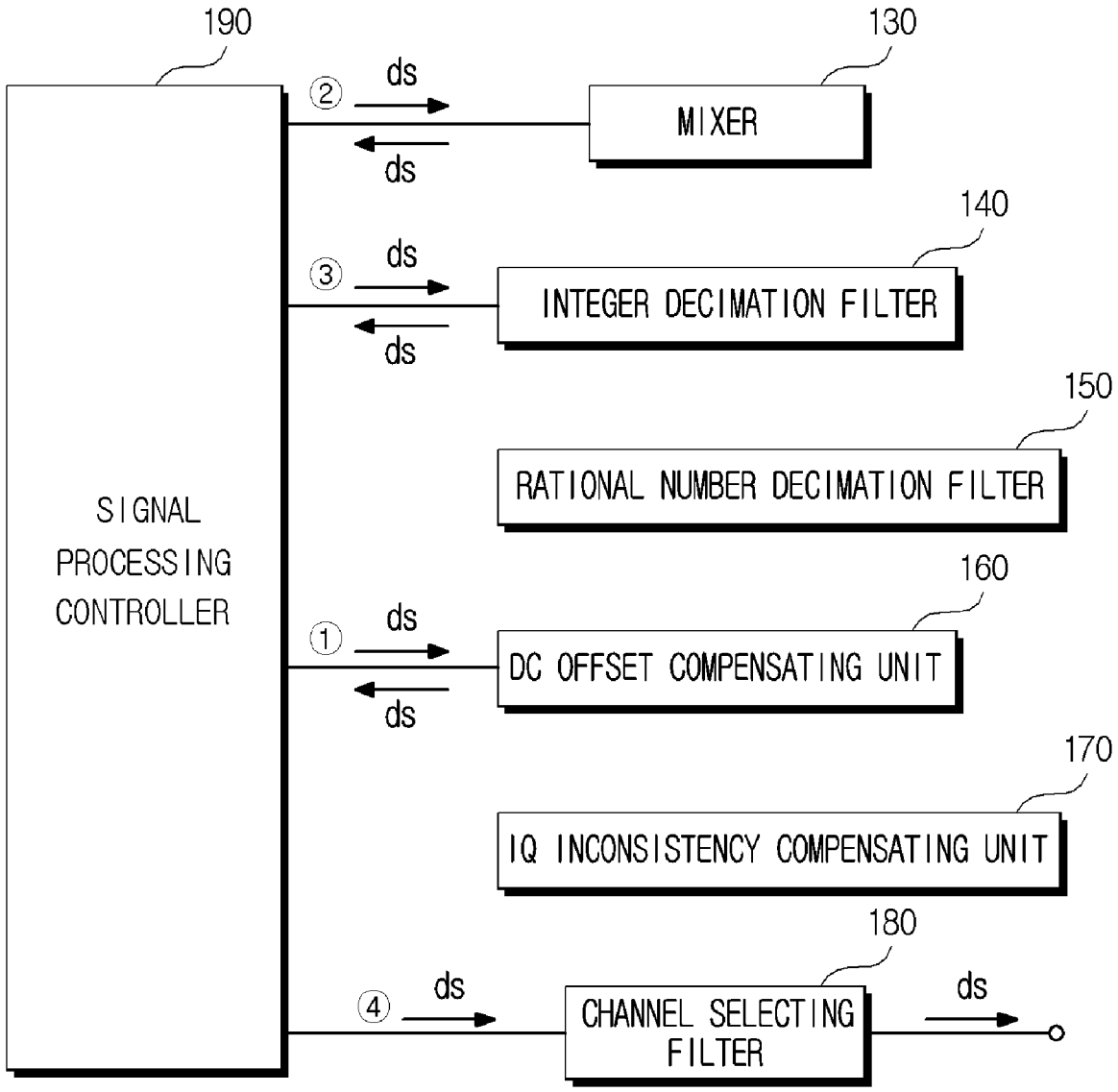
190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
ds
①
②
③
④

FIG.4B

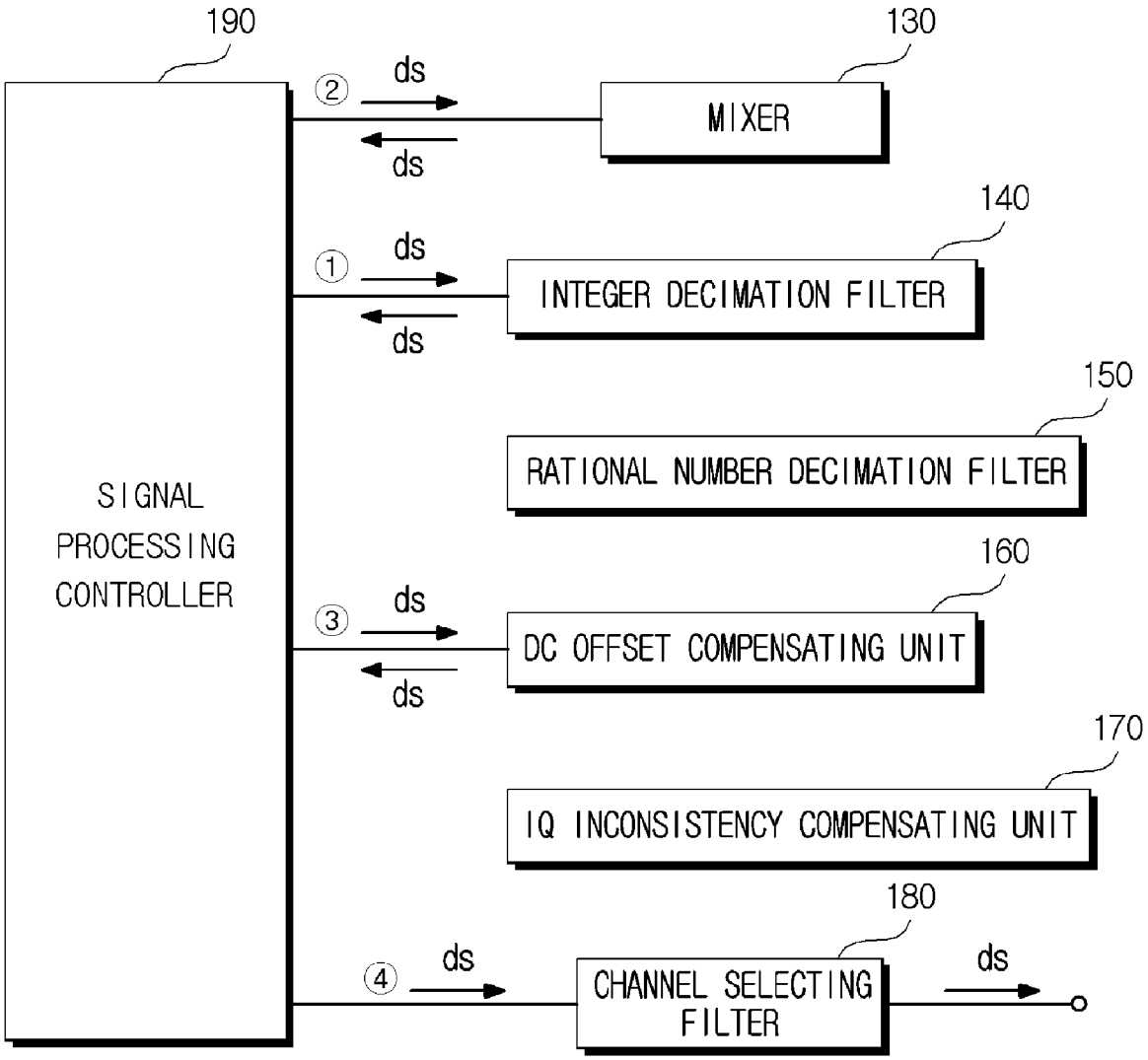
190
SIGNAL PROCESSING CONTROLLER
②
ds
ds
130
MIXER
①
ds
ds
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
③
ds
ds
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
④
ds
180
CHANNEL SELECTING FILTER
ds

FIG.5A

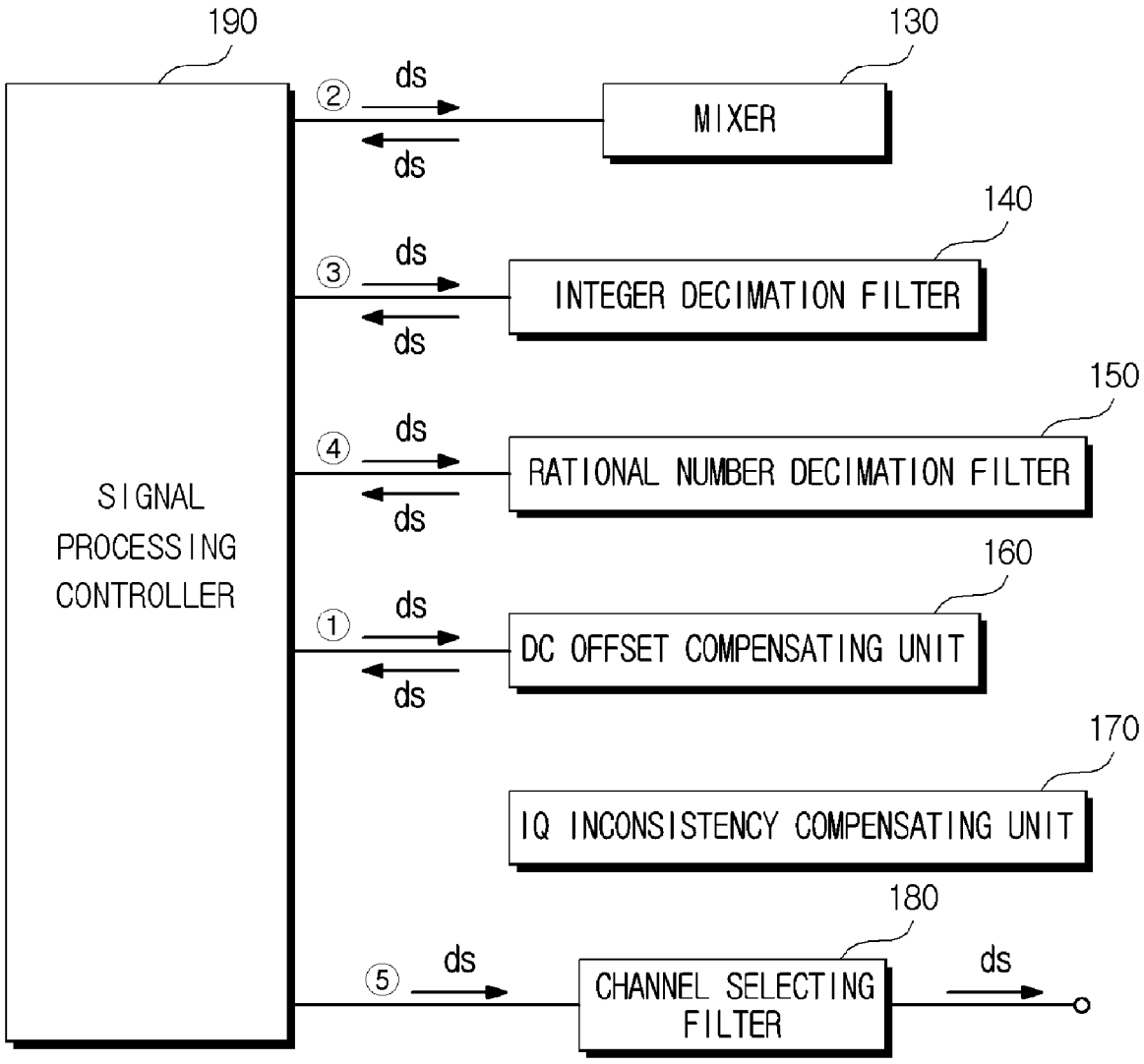
190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
ds
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FIG.5B

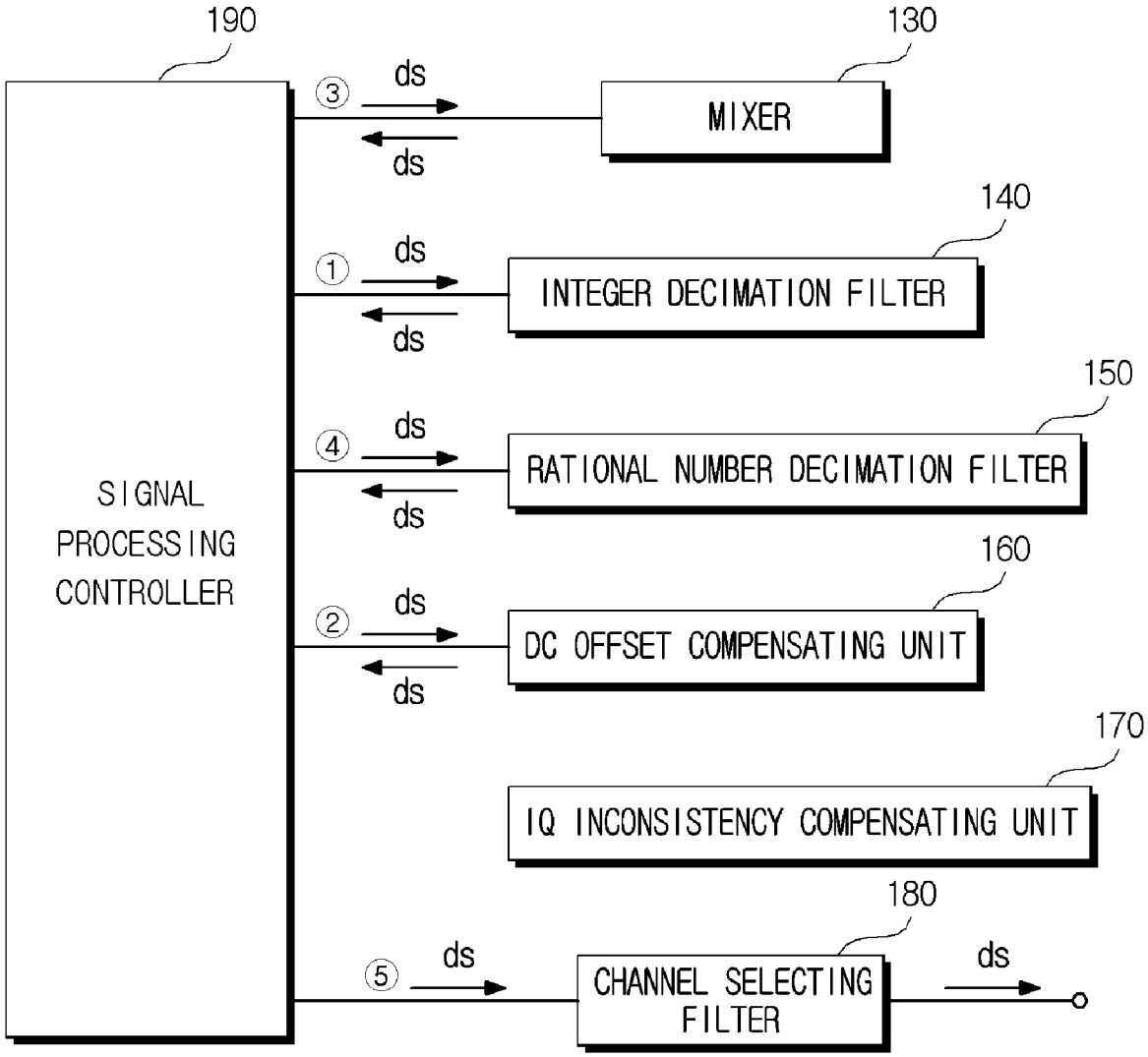
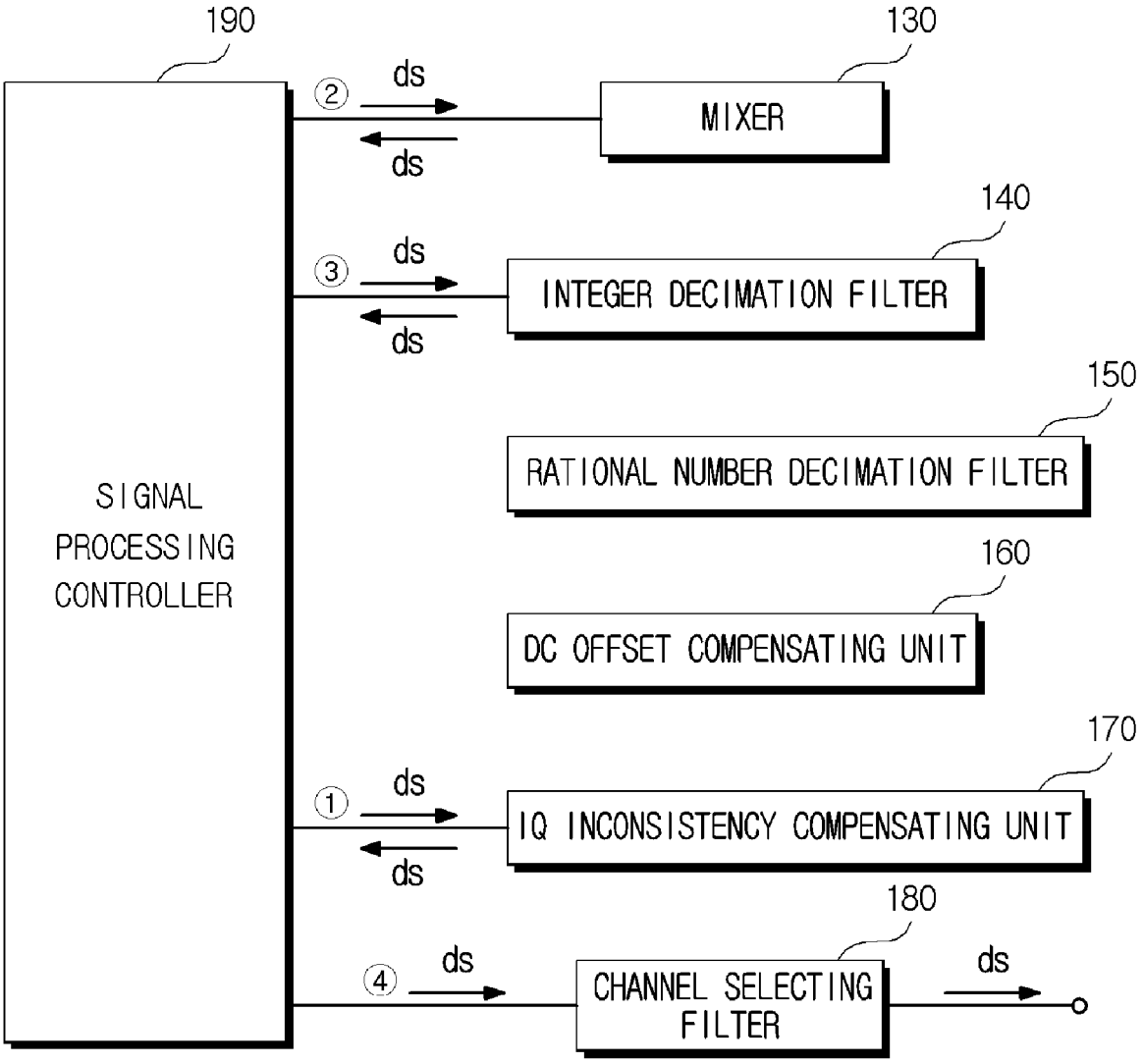

190
SIGNAL PROCESSING CONTROLLER
③ ds
ds
130
MIXER
① ds
ds
140
INTEGER DECIMATION FILTER
④ ds
ds
150
RATIONAL NUMBER DECIMATION FILTER
② ds
ds
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
⑤ ds
180
CHANNEL SELECTING FILTER
ds

FIG.6A


190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
ds
①
②
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④

FIG.6B

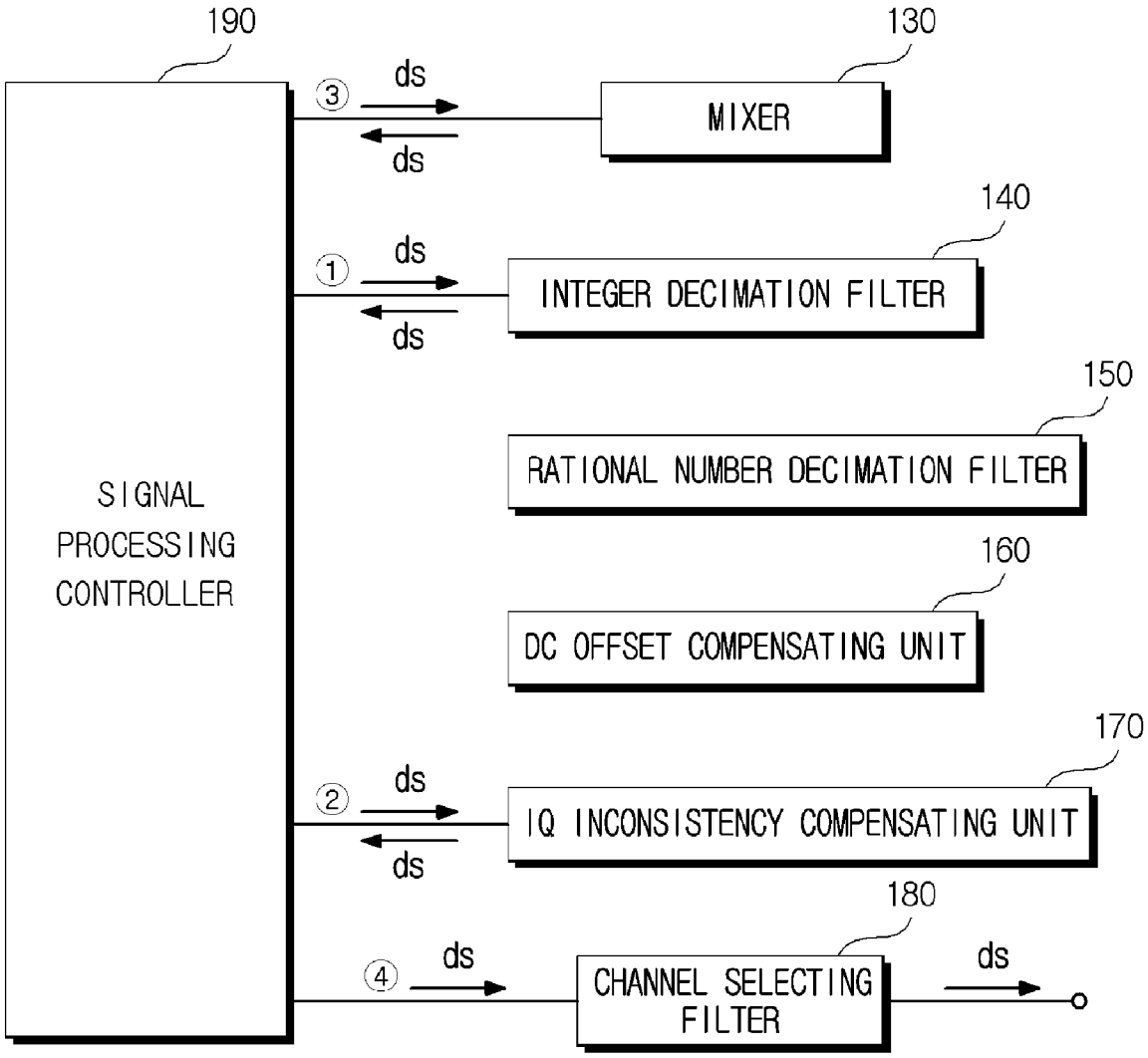
190
SIGNAL PROCESSING CONTROLLER
③
ds
ds
130
MIXER
①
ds
ds
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
②
ds
ds
170
IQ INCONSISTENCY COMPENSATING UNIT
④
ds
180
CHANNEL SELECTING FILTER
ds

FIG.7A

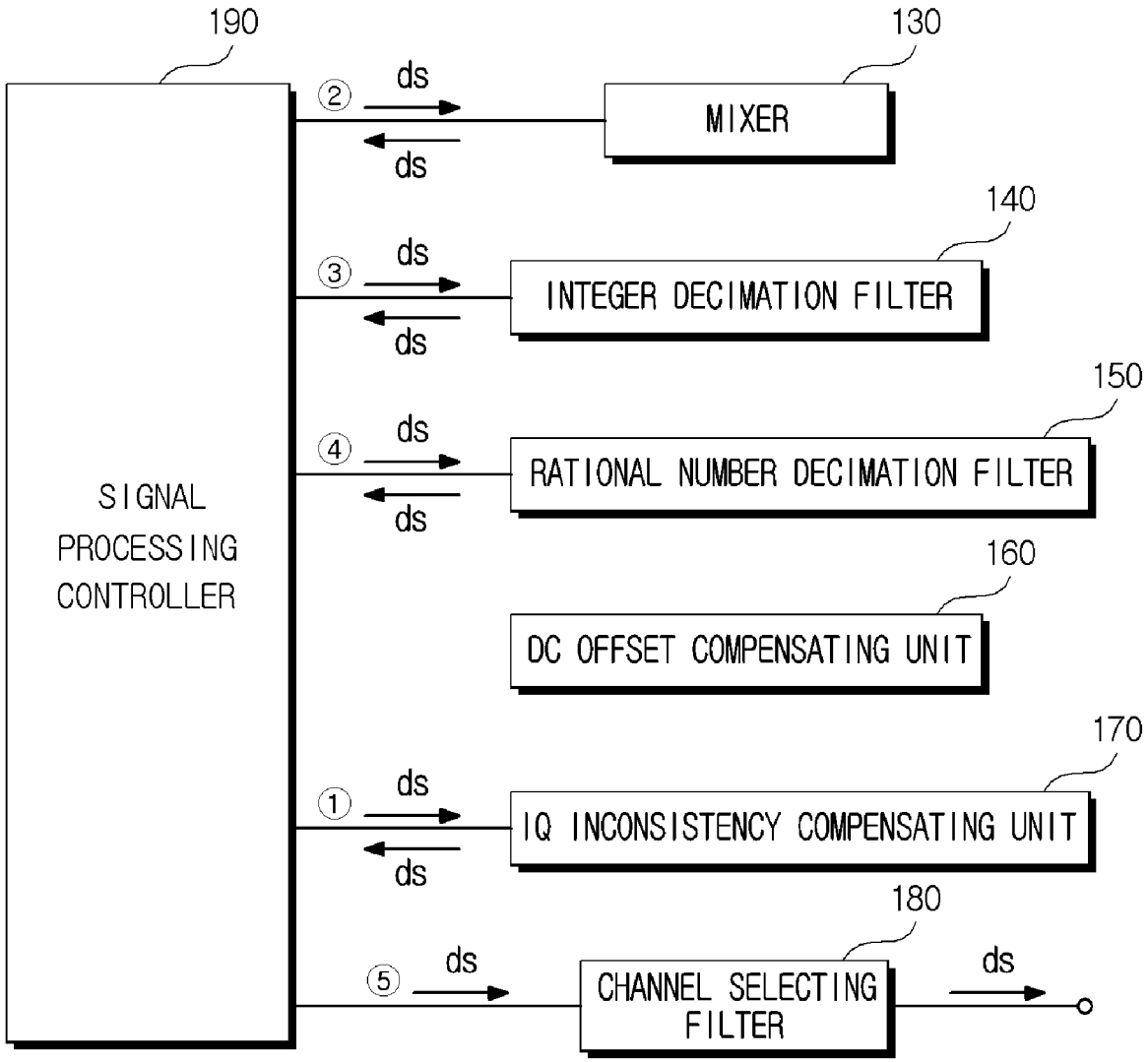
190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
ds
①
②
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FIG.7B

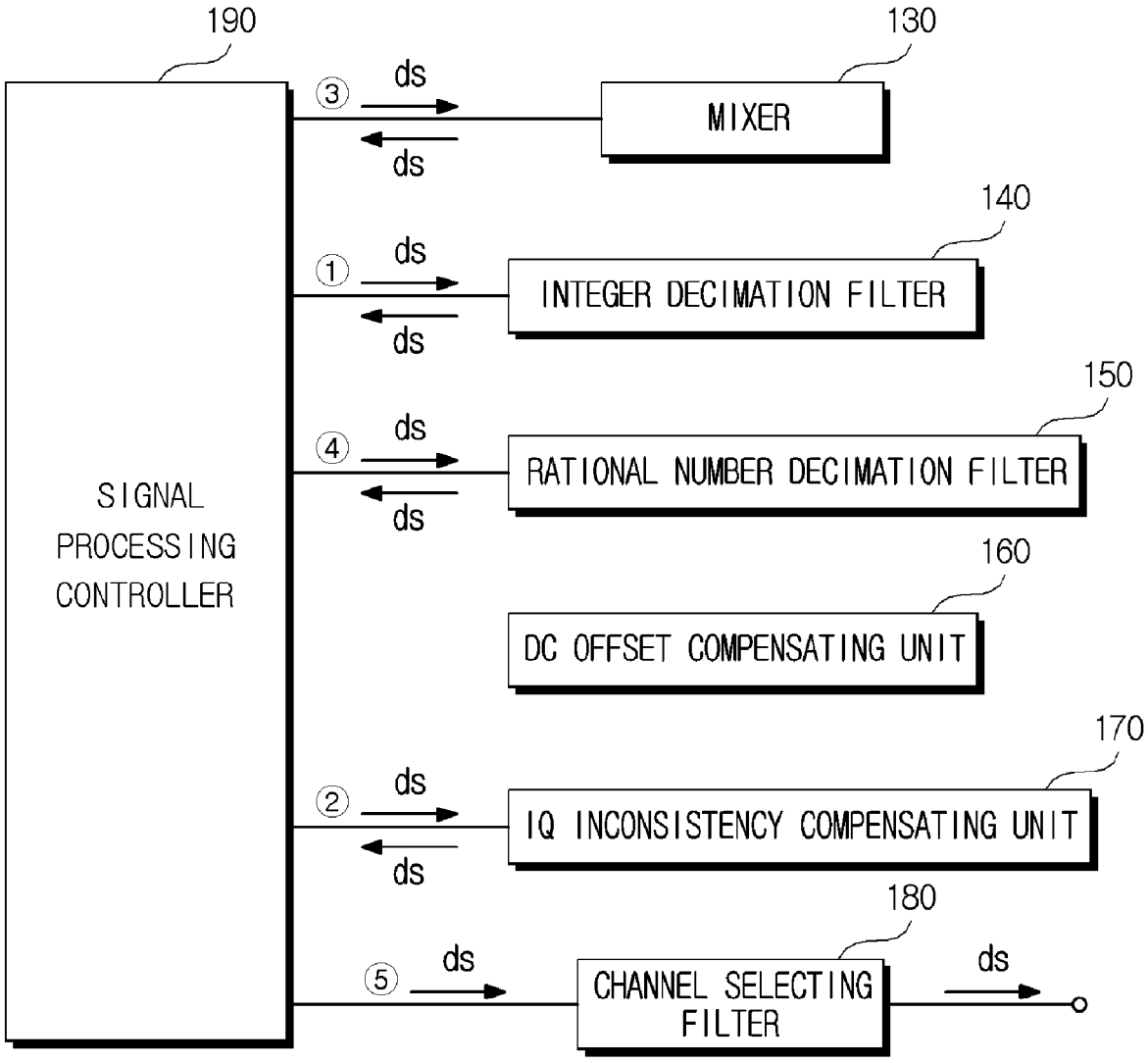
190
SIGNAL PROCESSING CONTROLLER
③ ds
ds
130
MIXER
① ds
ds
140
INTEGER DECIMATION FILTER
④ ds
ds
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
② ds
ds
170
IQ INCONSISTENCY COMPENSATING UNIT
⑤ ds
180
CHANNEL SELECTING FILTER
ds

FIG.8

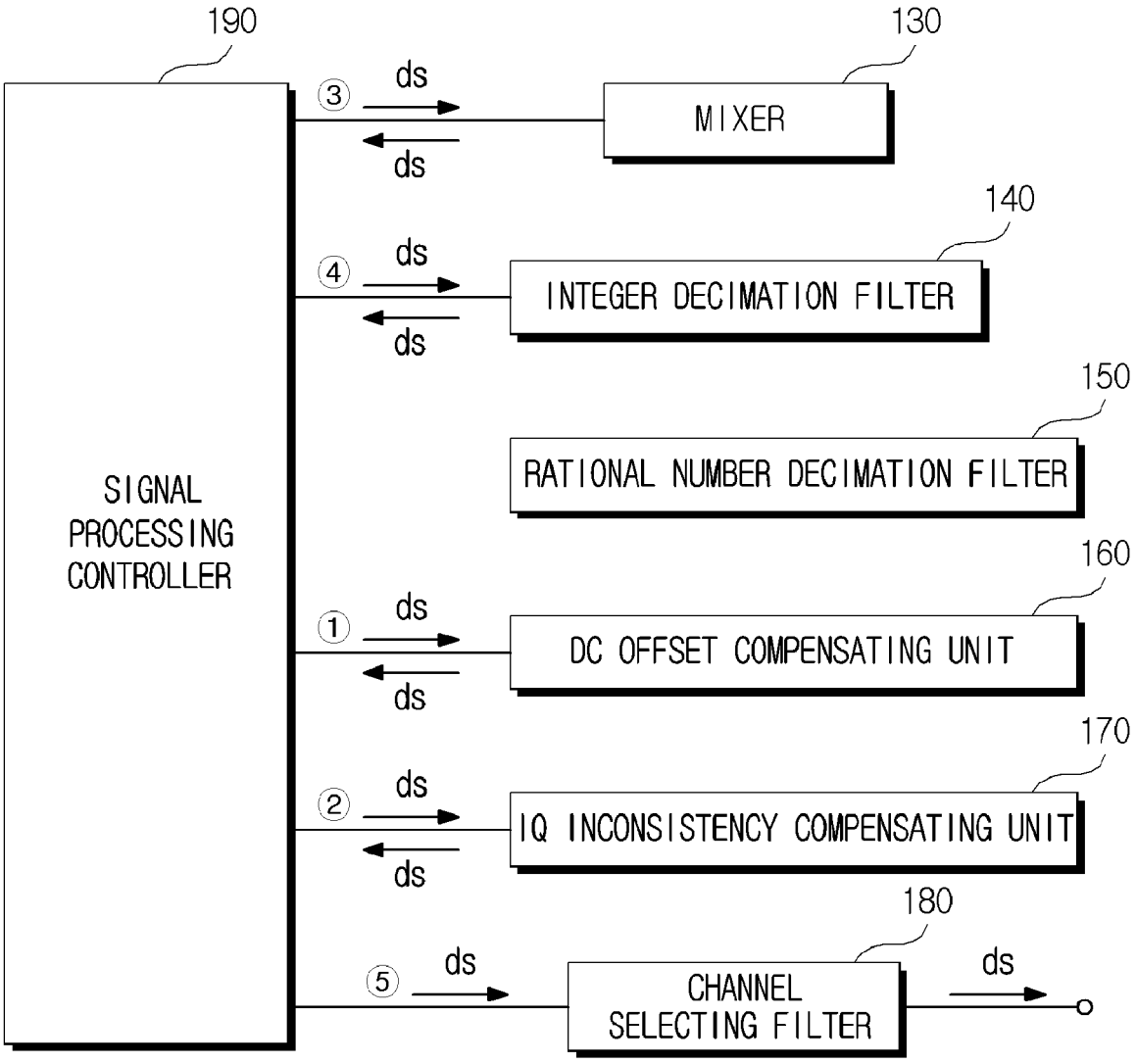
190
SIGNAL PROCESSING CONTROLLER
③ ds
ds
130
MIXER
④ ds
ds
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
① ds
ds
160
DC OFFSET COMPENSATING UNIT
② ds
ds
170
IQ INCONSISTENCY COMPENSATING UNIT
⑤ ds
180
CHANNEL SELECTING FILTER
ds

FIG.9

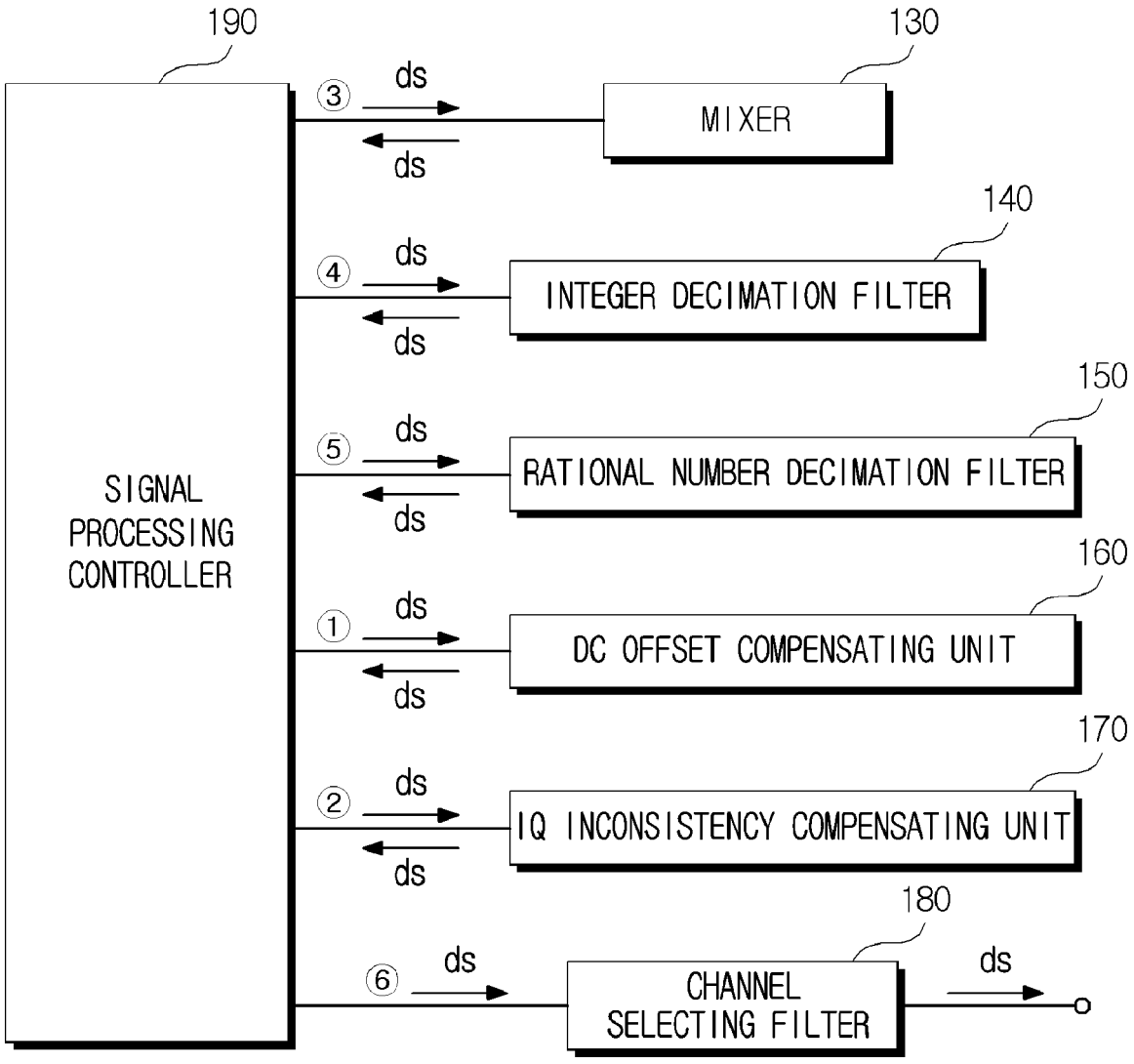
190
SIGNAL PROCESSING CONTROLLER
③ ds
ds
130
MIXER
④ ds
ds
140
INTEGER DECIMATION FILTER
⑤ ds
ds
150
RATIONAL NUMBER DECIMATION FILTER
① ds
ds
160
DC OFFSET COMPENSATING UNIT
② ds
ds
170
IQ INCONSISTENCY COMPENSATING UNIT
⑥ ds
180
CHANNEL SELECTING FILTER
ds

FIG.10A

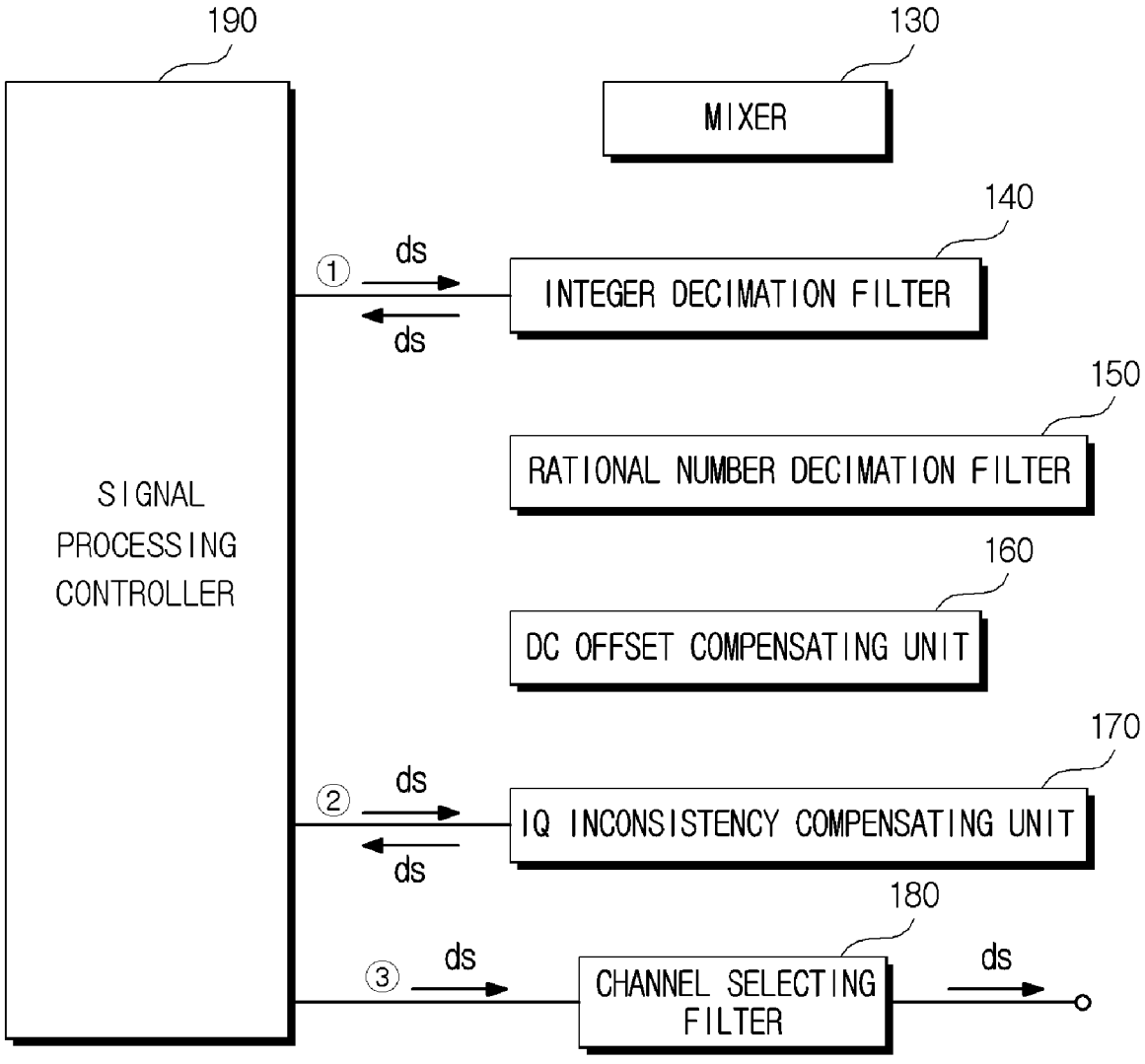
190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
① ds
ds
② ds
ds
③ ds
ds

FIG.10B

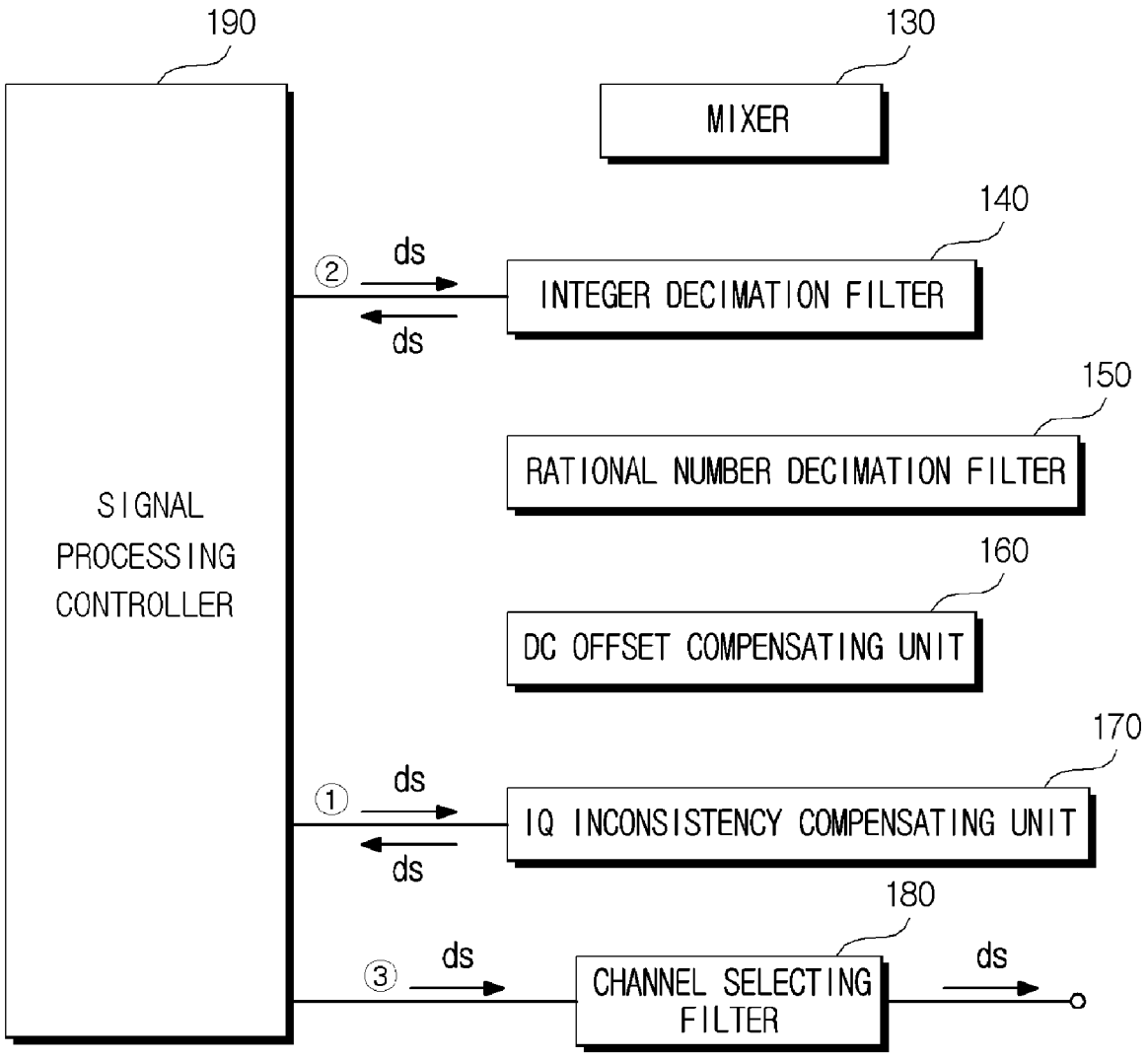
190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
ds
ds
ds
ds
ds
ds
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FIG.11A

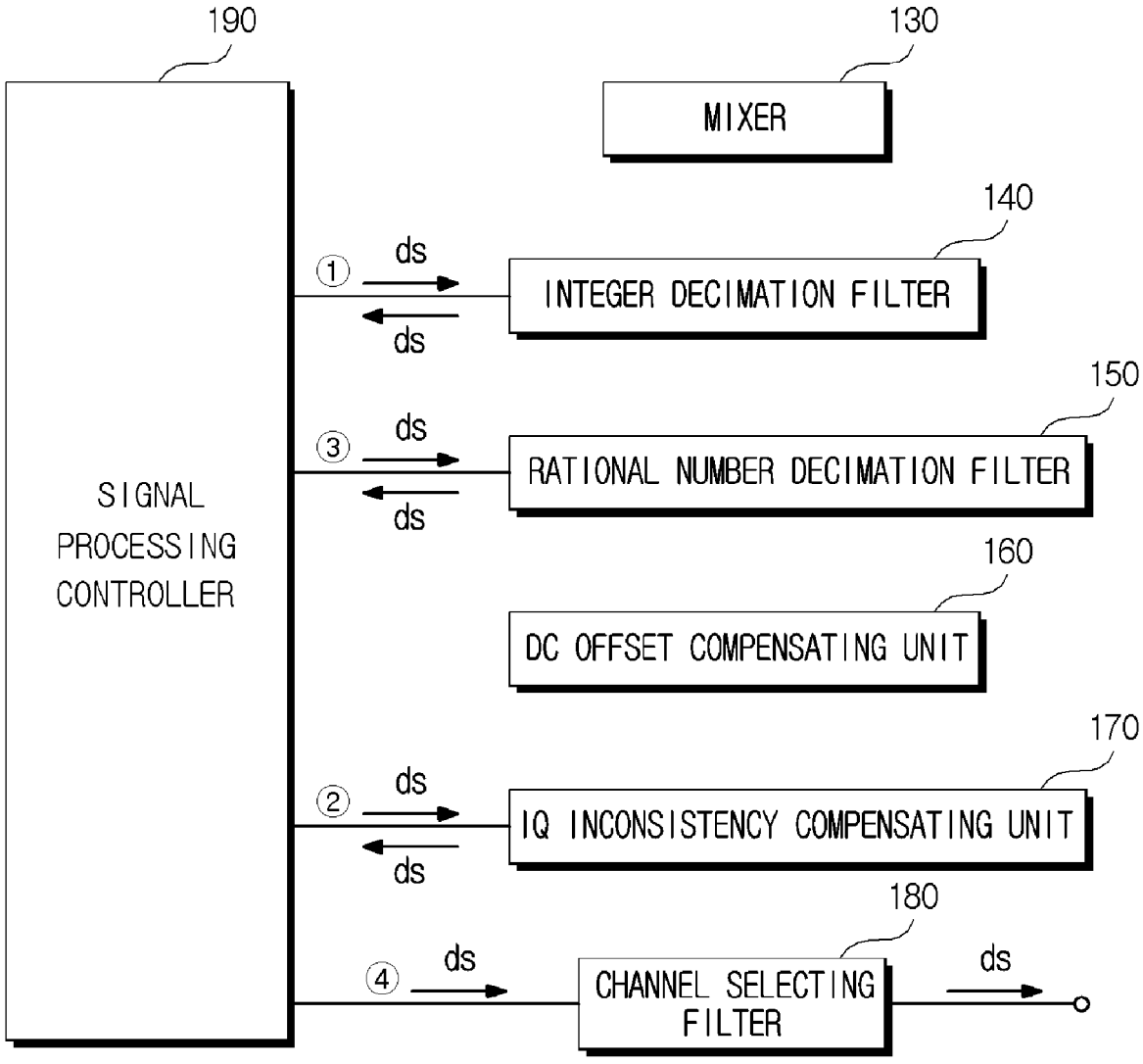
190
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
SIGNAL PROCESSING CONTROLLER
① ds ds
② ds ds
③ ds ds
④ ds
ds

FIG.11B

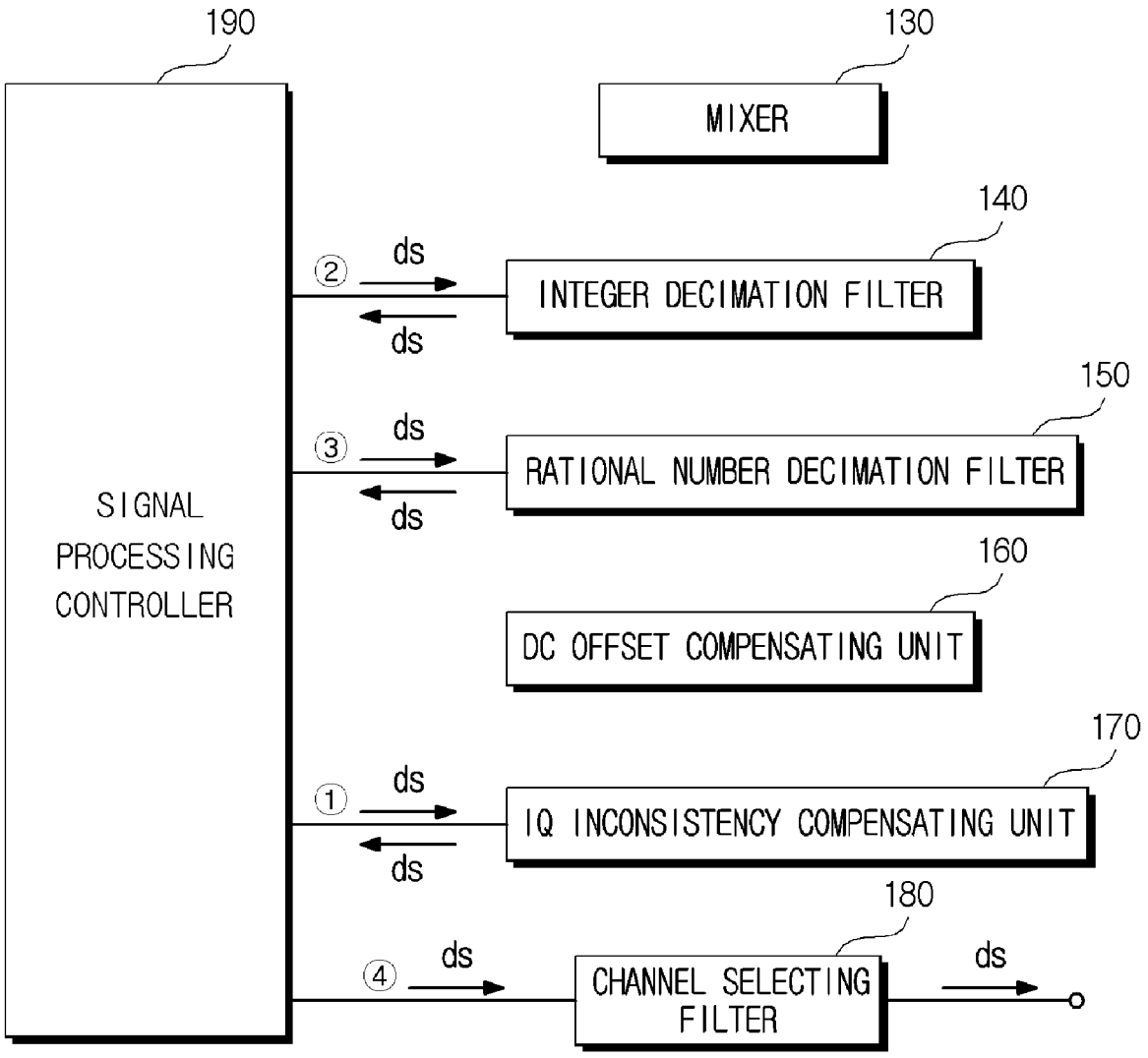
190
130
MIXER
140
ds
②
INTEGER DECIMATION FILTER
ds
150
ds
③
RATIONAL NUMBER DECIMATION FILTER
ds
SIGNAL
PROCESSING
CONTROLLER
160
DC OFFSET COMPENSATING UNIT
170
ds
①
IQ INCONSISTENCY COMPENSATING UNIT
ds
180
④
ds
CHANNEL SELECTING
FILTER
ds

FIG.12A

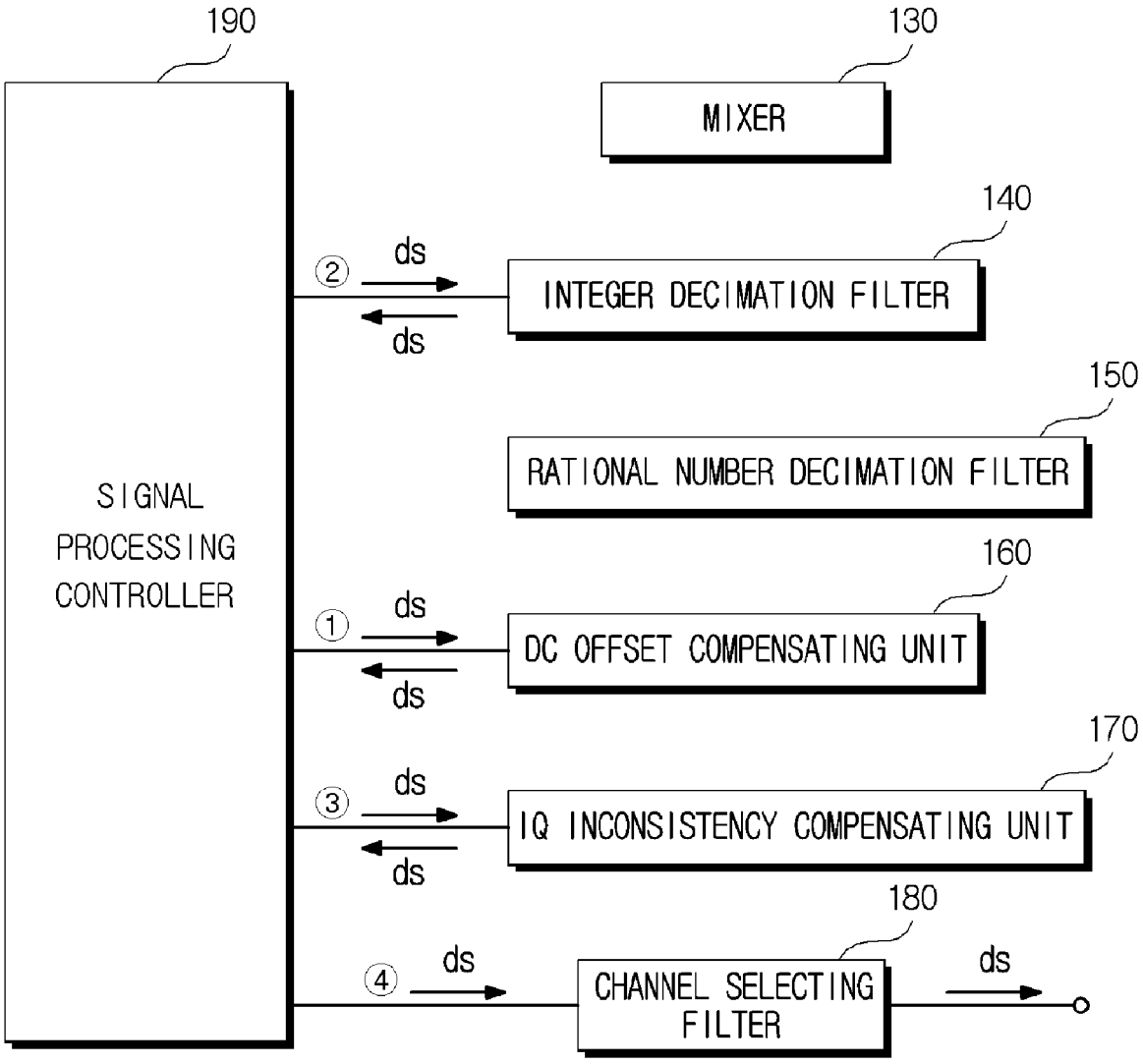
190
130
MIXER
140
②
ds
ds
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
SIGNAL PROCESSING CONTROLLER
160
①
ds
ds
DC OFFSET COMPENSATING UNIT
170
③
ds
ds
IQ INCONSISTENCY COMPENSATING UNIT
180
④
ds
CHANNEL SELECTING FILTER
ds

FIG.12B

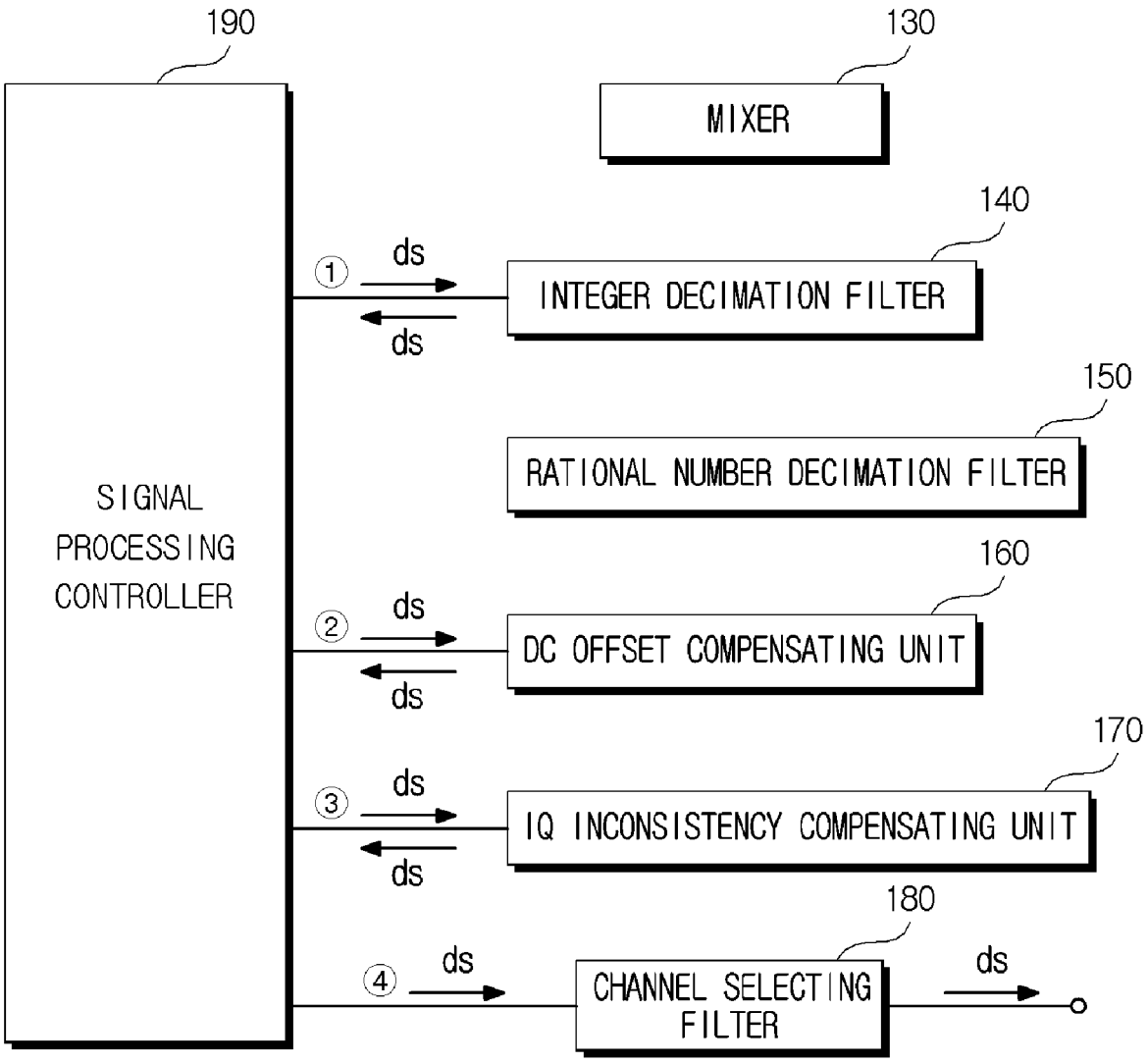
190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
① ds
ds
② ds
ds
③ ds
ds
④ ds
ds

FIG.13A

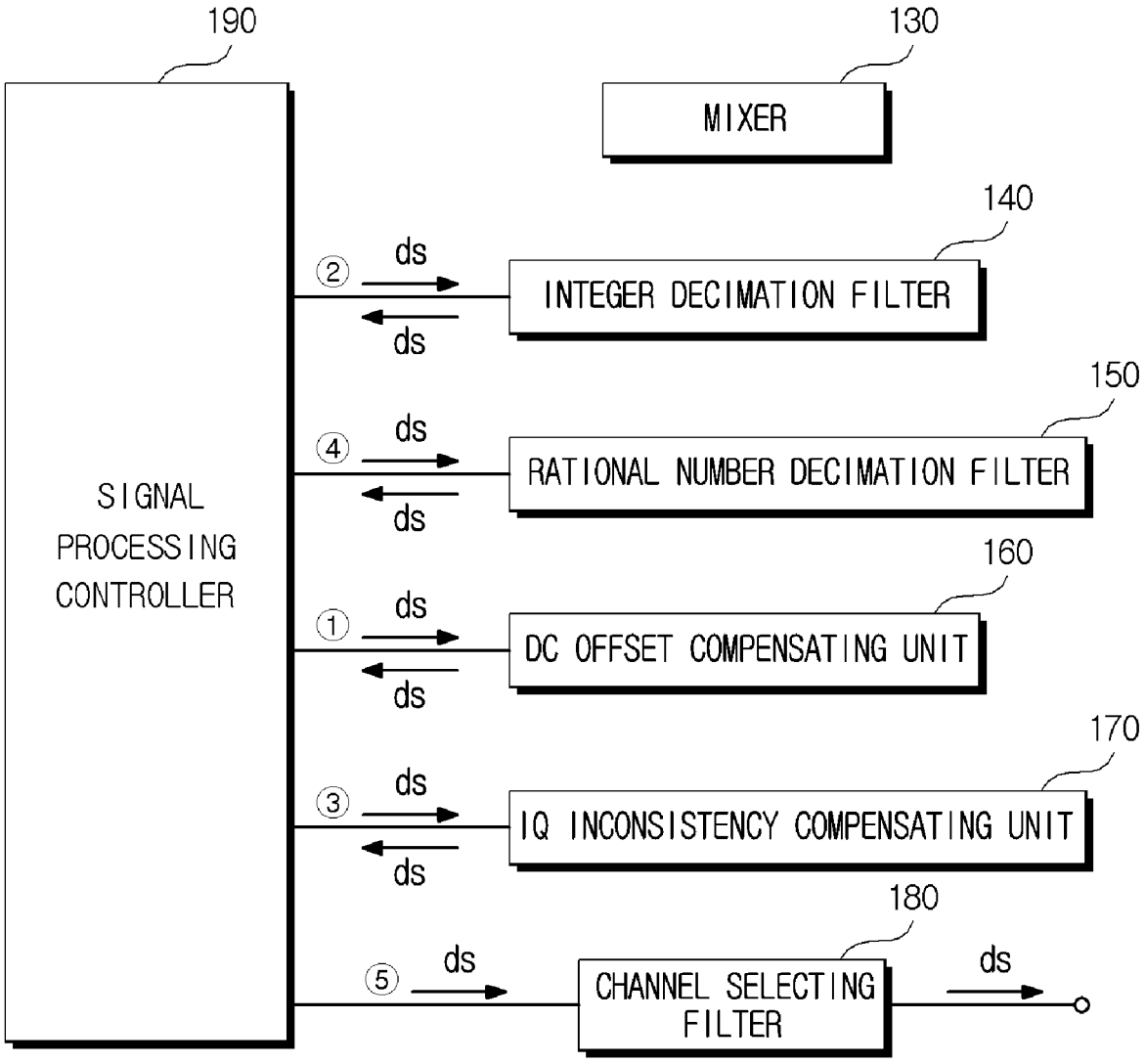
190
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
SIGNAL PROCESSING CONTROLLER
ds
①
②
③
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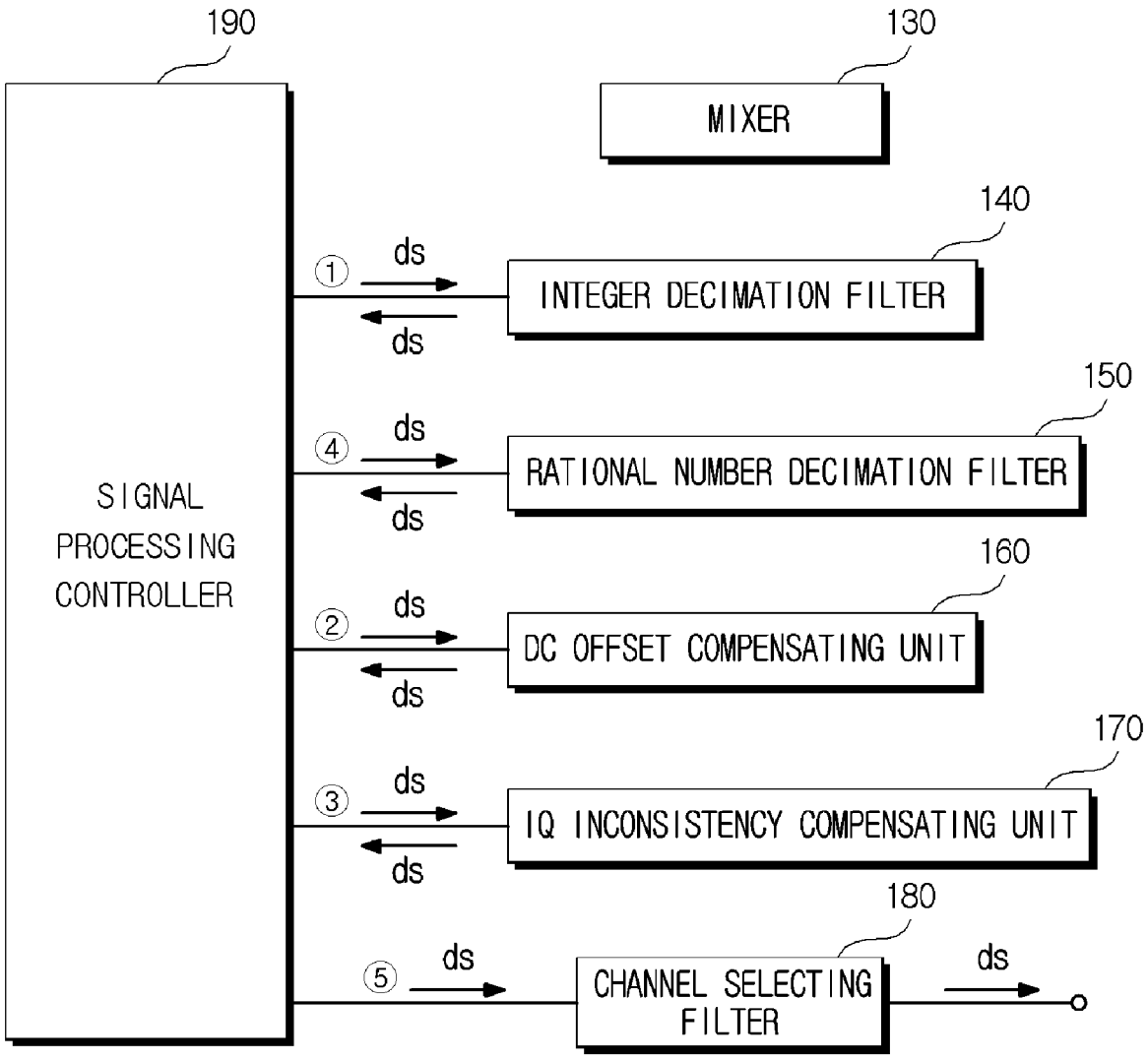
FIG.13B


190
SIGNAL PROCESSING CONTROLLER
130
MIXER
140
INTEGER DECIMATION FILTER
150
RATIONAL NUMBER DECIMATION FILTER
160
DC OFFSET COMPENSATING UNIT
170
IQ INCONSISTENCY COMPENSATING UNIT
180
CHANNEL SELECTING FILTER
① ds ds
④ ds ds
② ds ds
③ ds ds
⑤ ds
ds

DIGITAL RF RECEIVER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to and the benefit of Korean Patent Application No. 10-2012-0086998 filed in the Korean Intellectual Property Office on Aug. 8, 2012, and Korean Patent Application No. 10-2013-0067367 filed in the Korean Intellectual Property Office on Jun. 12, 2013, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

Embodiments relate to a digital RF receiver, and more particularly, to a digital RF receiver which easily receives a multiple mode of a wireless mobile communication receiving terminal, an MIMO, and an RF signal which supports change in a bandwidth expansion.

BACKGROUND ART

Generally, the RF receiver is a device which converts an RF signal received through an antenna into a signal band in which the RF signal is receivable at a lower level.

Such an RF receiver receives the RF signal through a duplexer and a mixer mixes an RF signal with a low noise amplified in a low noise amplifier and a local frequency supplied from a local frequency generator to generate an IF (intermediate frequency) signal and then pass only a desired band through a filter.

However, in the case of the RF receiver, when a new standard and a band and a bandwidth are newly added in accordance with the new standard, it needs lots of improvement time and cost to apply an RF receiving chip which is developed through new designing and manufacturing processes of an analog technology of the related art and manufacturing processes into a terminal.

Moreover, when a terminal which supports multiple modes is manufactured, a plurality of chips which supports individual standards is used in one terminal, which may increase a volume and a power consumption of the terminal.

Therefore, in recent years, studies are performed to develop an RF receiver which supports multiple mode reception, MIMO reception, and bandwidth expansion change using one RF receiving chip in one terminal.

SUMMARY OF THE INVENTION

The present invention has been made in an effort to provide a digital RF receiver which increases a reception performance in accordance with a noise signal included in RF signals which are input in different positions for every functional block in accordance with a mode and a bandwidth and a sampling rate and reduces power consumption for multiple mode reception, MIMO reception, and bandwidth expansion reception.

An exemplary embodiment of the present invention provides a digital RF receiver including a signal converting unit which converts an RF signal received from an external device into a digital signal, a plurality of functional modules which processes the digital signal in accordance with a predetermined algorithm when the digital signal is input, and a signal processing controller which selects at least one of the plurality of functional modules to control the digital signal to be processed in consideration of whether an IF signal component is included in the digital signal or a sampling rate related with sampling information of the digital signal.

The digital RF receiver varies a signal processing order for the RF signal in accordance with an input signal condition of the RF signal when the RF signal is received to reduce the power consumption and processing time to process the RF signal.

Further, the digital RF receiver varies the signal processing order for the RF signal in accordance with the input signal condition of the RF signal when the RF signal is received, to increase a flexibility of the receiver using a multiple mode, a MIMO, a bandwidth expansion receiver, and a simultaneous multiple mode.

The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustrating a control configuration of a digital RF receiver according to an exemplary embodiment.

FIGS. **2**A and **2**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a first exemplary embodiments.

FIGS. **3**A and **3**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a second exemplary embodiments.

FIGS. **4**A and **4**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a third exemplary embodiments.

FIGS. **5**A and **5**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a fourth exemplary embodiments.

FIGS. **6**A and **6**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a fifth exemplary embodiments.

FIGS. **7**A and **7**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a sixth exemplary embodiments.

FIG. **8** is a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a seventh exemplary embodiment.

FIG. **9** is a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to an eighth exemplary embodiment.

FIGS. **10**A and **10**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a ninth exemplary embodiments.

FIGS. **11**A and **11**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a tenth exemplary embodiments.

FIGS. **12**A and **12**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to an eleventh exemplary embodiments.

FIGS. **13**A and **13**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a twelfth exemplary embodiments.

It should be understood that the appended drawings are not necessarily to scale, presenting a somewhat simplified repre-

sentation of various features illustrative of the basic principles of the invention. The specific design features of the present invention as disclosed herein, including, for example, specific dimensions, orientations, locations, and shapes will be determined in part by the particular intended application and use environment.

In the figures, reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawing.

DETAILED DESCRIPTION

The following description illustrates only a principle of the present invention. Therefore, those skilled in the art may implement the principle of the present invention and invent various apparatuses, which are included in a concept and a scope of the present invention, even though not clearly described or illustrated in the specification. It should be understood that all conditional terms and exemplary embodiments, which are described in the specification, are clearly intended only to understand the concept of the invention, but the present invention is not limited to the exemplary embodiments and states as described above.

Further, it should be understood that all detailed description, which specifies not only a principle, an aspect, and an exemplary embodiment, but also a specific exemplary embodiment, is intended to include structural and functional equivalents. It should be understood that such equivalents include all elements which are invented so as to perform the same function as the currently disclosed equivalents and equivalents, which will be developed in the future, regardless with the structure.

Therefore, for example, the block diagram of the present specification should be understood to represent an illustrative conceptual aspect which specifies the principle of the invention. Similarly, it should be understood that all of a flowchart, a status transitional view, and a pseudo code may be substantially represented in a computer readable medium and indicate various processes executed by a computer or a processor regardless of whether the computer or the processor is apparently illustrated.

Functions of various elements illustrated in the drawings including a functional block, which is represented by a processor or a concept similar thereto, may be provided by using not only an exclusive hardware but also a hardware which may execute a software with regard to an appropriate software. If the function is provided by the processor, the function may be provided by a single exclusive processor, a single shared processor or a plurality of individual processors, and some of them may be shared.

Further, a precise usage of a processor, control or a terminology suggested as a concept similar thereto should not be interpreted by exclusively citing hardware, which is capable of executing software, but should be understood to implicatively include a digital signal processor (DSP), and a ROM, a RAM, and a nonvolatile memory which store hardware and software without any restrictions. Widely known and commonly used other hardware may also be included therein.

In claims of this specification, components represented as means to perform the function described in the detailed description are intended to include, for example, a combination of circuit elements which perform the above-mentioned functions or all methods which performs functions including all types of software including a firmware/microcode, and are combined with an appropriate circuit which executes the software in order to perform the function. In the invention defined by the claims, the functions provided by the variously described means are combined with each other and combined with the method demanded by the claims so that any means which may provide the above-mentioned function should be understood to be equivalent to be understood from the specification.

The above objects, features, and advantages will be more obvious from the detailed description with reference to the accompanying drawings, and accordingly, those skilled in the art to which the invention pertains will be able to easily implement the technical spirit of the invention. However, in describing the present invention, if it is considered that description of a related known technology may unnecessarily cloud the gist of the present invention, the description thereof will be omitted.

Hereinafter, an exemplary embodiment of the present invention will be described in detail with reference to the accompanying drawings.

FIG. **1** is a block diagram illustrating a control configuration of a digital RF receiver according to an exemplary embodiment.

Referring to FIG. **1**, the digital RF receiver may include a low noise amplifier **110**, a signal converting unit **120**, a plurality of functional modules (not illustrated), and a signal processing controller **190**.

The low noise amplifier **110** amplifies an RF signal s which is received by an antenna (not illustrated) to have a predetermined amplitude.

Here, the low noise amplifier **110** suppresses the amplification of a noise component included in the RF signal s and adjusts an amplitude of the RF signal s to be output. In this case, the low noise amplifier **110** functions as a band limiting filter which removes the superposition of the noise component in the signal converting unit **120** in advance.

In the exemplary embodiment, the RF signal s has different bands and different bandwidths in accordance with the standards and may have multiple bands and bandwidths even in one standard, but the invention is not limited thereto. Further, the RF signal s may adopt a multiple antenna transceiving (MIMO) technique and a bandwidth expansion technique which simultaneously sends a signal to several bands in order to increase a signal transmission rate, but the invention is not limited thereto.

The signal converting unit **120** converts an RF signal s output from the low noise amplifier **110** into a digital signal ds.

And, the signal converting unit **120** may occur separated of an In-phase signal and a quadrature signal from the digital signal ds, but the invention is not limited thereto.

The plurality of functional modules may include a mixer **130**, an integer decimation filter **140**, a rational number decimation filter **150**, a DC offset compensating unit **160**, an IQ inconsistency compensating unit **170**, and a channel selecting filter **180**.

Here, when a digital signal ds is input, the mixer **130** may remove an IF (intermediate frequency) signal included in the digital signal ds and/or separate a phase.

The mixer **130** may occur separated of an In-phase signal and a quadrature signal from the digital signal ds and/or may be function a carrier shift of the digital signal ds.

The integer decimation filter **140** may perform integer decimation so as to satisfy an integer sampling rate which is required in an arbitrary standard which generates an RF signal s.

The rational number decimation filter **150** may perform rational number decimation so as to satisfy a rational number sampling rate which is required in an arbitrary standard.

When the digital signal ds is input, the DC offset compensating unit **160** may remove a DC component included in the digital signal ds.

Here, when the digital signal ds is input, the IQ inconsistency compensating unit **170** compensates a phase error of an In-phase signal and a quadrature signal from the digital signal ds.

When the digital signal ds is input, the channel selecting filter **180** may remove an interference signal in an adjacent band from the digital signal ds.

When the digital signal ds is input, the signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with the input signal condition of the RF signal s to control the digital signal ds to be processed.

That is, the signal processing controller **190** inputs the digital signal ds to any one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** and receives the digital signal ds output from the any one of the mixer **130**, the integer decimation filter **140**, a rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to transmit the digital signal ds to another one and repeats the above operation selected at least two times to control the digital signal ds to be processed.

The digital RF receiver according to the exemplary embodiment is connected to the signal processing controller **190**, separately from the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** so that the signal processing controller **190** determines an order of processing the digital signal ds to control the digital signal ds to be processed.

In the exemplary embodiment, the arbitrary signal which is input to the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** may be a digital signal ds output from the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** but the invention is not limited thereto.

FIGS. **2**A and **2**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a first exemplary embodiments.

In FIGS. **2**A and **2**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configuration will be briefly described.

Referring to FIGS. **2**A and **2**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds to control the digital signal ds as illustrated in FIG. **1** to be processed.

Here, referring to FIG. **2**A, in the input signal condition where the digital signal ds includes an IF signal and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the mixer **130**, the integer decimation filter **140**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds which is transmitted from the signal converting unit **120**, to the mixer **130** from the mixer **130**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the mixer **130**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

In this case, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal from the transmitted digital signal ds to a decoder (not illustrated) or other processing device.

Here, the interference signal may be an original noise signal of and an inflow noise signal in at least one of the mixer **130**, the integer decimation filter **140**, and the signal processing controller **190**, but the invention is not limited thereto. The original noise signal included in the RF signal.

Here, referring to FIG. **2**B, in the input signal condition where the digital signal ds includes an IF signal and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the mixer **130**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **2**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **2**A.

Differently from FIG. **2**A, in FIG. **2**B, after performing the integer decimation on a digital signal ds first in the integer decimation filter **140**, the IF signal is removed to separate a phase in the mixer **130** and then the digital signal is transmitted to the channel selecting filter **180**.

In FIGS. **2**A and **2**B, the signal processing controller **190** selects the mixer **130**, the integer decimation filter **140**, and the channel selecting filter **180** and inputs the digital signal ds to the mixer **130**, the integer decimation filter **140**, and the channel selecting filter **180**. However, the signal processing controller **190** may input the digital signal ds to any one of the mixer **130**, the integer decimation filter **140**, and the channel selecting filter **180** to control the digital signal ds to be continuously input in accordance with the predetermined signal processing order.

FIGS. **3**A and **3**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a second exemplary embodiments.

In FIGS. **3**A and **3**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIGS. **3**A and **3**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compen-

sating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **3**A, in the input signal condition where the digital signal ds includes an IF signal and a rational number sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds which is transmitted from the signal converting unit **120** to the mixer **130** and receives the digital signal ds in which the IF signal included in the digital signal ds is removed and/or a phase is separated, from the mixer **130**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the mixer **130**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

Thereafter, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the rational number decimation filter **150** and the rational number decimation filter **150** transmits the rational number-decimated digital signal ds to the signal processing controller **190**.

In this case, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the rational number decimation filter **150**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **3**B, in the input signal condition where the digital signal ds includes an IF signal and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the mixer **130**, the rational number decimation filter **150**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **3**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **3**A.

Differently from FIG. **3**A, in FIG. **3**B, after performing the integer decimation on a digital signal ds first in the integer decimation filter **140**, the IF signal is removed to separate a phase in the mixer **130**, the digital signal is rational number-decimated in the rational number decimation filter **150**, and then is transmitted to the channel selecting filter **180**.

In FIGS. **3**A and **3**B, even though it is described that the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, and the channel selecting filter **180**, but controls the digital signal ds to be automatically transmitted to the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, and the channel selecting filter **180** in accordance with the set signal processing order. However, the invention is not limited thereto.

FIGS. **4**A and **4**B are a block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a third exemplary embodiments.

In FIGS. **4**A and **4**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIGS. **4**A and **4**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **4**A, in the input signal condition where the digital signal ds includes an IF signal and a DC component and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the DC offset compensating unit **160**, the mixer **130**, the integer decimation filter **140**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the DC offset compensating unit **160** and the DC offset compensating unit **160** transmits a digital signal ds in which a DC component included in the digital signal ds is removed to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the DC offset compensating unit **160**, to the mixer **130** and receives the digital signal ds in which the IF signal included in the digital signal ds is removed and/or a phase is separated, from the mixer **130**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the mixer **130**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

Thereafter, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the mixer **130**,

the integer decimation filter **140**, the DC offset compensating unit **160**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **4**B, in the input signal condition where the digital signal ds includes an IF signal and a DC component and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the mixer **130**, the DC offset compensating unit **160**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **4**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **4**A.

Differently from FIG. **4**A, in FIG. **4**B, after performing the integer decimation on a digital signal ds first in the integer decimation filter **140**, the IF signal is removed in the mixer **130**, and then the digital signal ds in which the DC component included in the digital signal ds is removed first in the DC offset compensating unit **160** is transmitted to the channel selecting filter **180**.

In FIGS. **4**A and **4**B, even though it is described that the mixer **130**, the integer decimation filter **140**, the DC offset compensating unit **160**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the mixer **130**, the integer decimation filter **140**, the DC offset compensating unit **160**, and the channel selecting filter **180**, but controls the digital signal to be automatically transmitted to the mixer **130**, the integer decimation filter **140**, the DC offset compensating unit **160**, and the channel selecting filter **180** in accordance with the set signal processing order However, the invention is not limited thereto.

FIGS. **5**A and **5**B are a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a fourth exemplary embodiments.

In FIGS. **5**A and **5**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or repeated configurations will be briefly described.

Referring to FIGS. **5**A and **5**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **5**A, in the input signal condition where the digital signal ds includes an IF signal and the DC component and a rational number sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the DC offset compensating unit **160**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the DC offset compensating unit **160** and the DC offset compensating unit **160** transmits a digital signal ds in which a DC component included in the digital signal ds is removed to the signal processing unit **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the DC offset compensating unit **160**, to the mixer **130**, and receives the digital signal ds in which the IF signal included in the digital signal ds is removed and a phase is separated, from the mixer **130**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the mixer **130**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

Thereafter, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the rational number decimation filter **150** and the rational number decimation filter **150** receives the rational number-decimated digital signal ds.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the rational number decimation filter **150**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the mixer **130**, the integer decimation filter **140**, the DC offset compensating unit **160**, the rational number decimation filter **150**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **5**B, in the input signal condition where the digital signal ds includes an IF signal and a DC component and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **160**, the mixer **130**, the DC offset compensating unit **160**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **5**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **5**A.

Differently from FIG. **5**A, in FIG. **5**B, the integer decimation is performed on a digital signal ds first in the integer decimation filter **140**, the DC component is removed in the DC offset compensating unit **160**, the IF signal is removed in the mixer **130** so that a digital signal ds is rational number-decimated in the rational number decimation filter **150**, and then is transmitted to the channel selecting filter **180**.

In FIGS. **5**A and **5**B, even though it is described that the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, and the channel selecting filter **180**, but controls the digital signal to be automatically transmitted to the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, and the channel

selecting filter **180** in accordance with the set signal processing order. However, the invention is not limited thereto.

FIGS. **6**A and **6**B are a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a fifth exemplary embodiments.

In FIGS. **6**A and **6**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or repeated configurations will be briefly described.

Referring to FIGS. **6**A and **6**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed. Here, referring to FIG. **6**A, in the input signal condition where the digital signal ds includes an IF signal, the IQs are inconsistent, and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the mixer **130**, the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the IQ inconsistency compensating unit **170** and the IQ inconsistency compensating unit **170** transmits a digital signal ds in which a phase error of an In-phase signal and a quadrature signal is compensated in the digital signal ds to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the IQ inconsistency compensating unit **170**, to the mixer **130** and receives the digital signal ds in which the IF signal included in the digital signal ds is removed and/or a phase is separated, from the mixer **130**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the mixer **130**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

Thereafter, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the mixer **130**, the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **6**B, in the input signal condition in which the digital signal ds includes an IF signal, the IQs are inconsistent, and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the mixer **130**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **6**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **6**A.

Differently from FIG. **6**A, in FIG. **6**B, the integer decimation is performed in the integer decimation filter **140**, the IQ inconsistency compensating unit **170** transmits a digital signal ds in which a phase error of an In-phase signal and the quadrature signal is compensated to the mixer **130**, and the IF signal is removed in the mixer **130** to transmit the digital signal ds to the channel selecting filter **180**.

In FIGS. **6**A and **6**B, even though it is described that the mixer **130**, the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the mixer **130**, the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180**, but controls the digital signal to be automatically transmitted to the mixer **130**, the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with the set signal processing order. However, the invention is not limited thereto.

FIGS. **7**A and **7**B are a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a sixth exemplary embodiments.

In FIGS. **7**A and **7**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIGS. **7**A and **7**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **7**A, in the input signal condition where the digital signal ds includes an IF signal, the IQs are inconsistent, and a rational number sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the IQ inconsistency compensating unit **170** and the IQ inconsistency compensating unit **170** transmits a digital signal ds in which a phase error of an In-phase signal and a quadrature signal is compensated in the digital signal ds to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the IQ inconsistency

compensating unit **170**, to the mixer **130** and receives the digital signal ds in which the IF signal included in the digital signal ds is removed and/or a phase is separated, from the mixer **130**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the mixer **130**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

Thereafter, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the rational number decimation filter **150**.

The rational number decimation filter **150** performs the rational number decimation on the digital signal ds to transmit the rational number-decimated digital signal to the signal processing controller **190** and the signal processing controller **190** transmits the digital signal ds transmitted from the rational number decimation filter **160** to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **7**B, in the input signal condition in which the digital signal ds includes an IF signal, the IQs are inconsistent, and a rational number sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the mixer **130**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **7**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **7**A.

Differently from FIG. **7**A, in FIG. **7**B, the integer decimation is performed on the digital signal ds in the integer decimation filter **140**, the digital signal ds in which a phase error of an In-phase signal and the quadrature signal is compensated in the IQ inconsistency compensating unit **170**, and the digital signal ds in which the IF signal is removed from the mixer **130** is rational number-decimated in the rational number decimation filter **150** and then transmitted to the channel selecting filter **180**.

In FIGS. **7**A and **7**B, even though it is described that the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180**, but controls the digital signal to be automatically transmitted to the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with the set signal processing order. However, the invention is not limited thereto.

FIG. **8** is a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a seventh exemplary embodiment.

In FIG. **8**, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIG. **8**, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **8**, in the input signal condition where the digital signal ds includes an IF signal and a DC component, the IQs are inconsistent, and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the mixer **130**, the integer decimation filter **140**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the DC offset compensating unit **160** and the DC offset compensating unit **160** transmits a digital signal ds in which a DC component included in the digital signal ds is removed to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the DC offset compensating unit **160**, to the IQ inconsistency compensating unit **170** and the IQ inconsistency compensating unit **170** transmits a digital signal ds in which a phase error of an In-phase signal and a quadrature signal is compensated in the digital signal ds to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the IQ inconsistency compensating unit **170**, to the mixer **130** and receives the digital signal ds in which the IF signal included in the digital signal ds is removed, from the mixer **130**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the mixer **130**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

Thereafter, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the mixer **130**, the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

FIG. **9** is a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to an eighth exemplary embodiment.

In FIG. **9**, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIG. **9**, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least two of the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **9**, in the input signal condition where the digital signal ds includes an IF signal and a DC component, the IQs are inconsistent, and a rational number sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the DC offset compensating unit **160** and the DC offset compensating unit **160** transmits a digital signal ds in which a DC component included in the digital signal ds is removed to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the DC offset compensating unit **160**, to the IQ inconsistency compensating unit **170** and the IQ inconsistency compensating unit **170** transmits a digital signal ds in which a phase error of an In-phase signal and a quadrature signal is compensated in the digital signal to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the IQ inconsistency compensating unit **170**, to the mixer **130** and receives the digital signal ds in which the IF signal included in the digital signal ds is removed, from the mixer **130**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the mixer **130**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

Thereafter, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the rational number decimation filter **150**.

The rational number decimation filter **150** transmits a rational number decimated digital signal ds in which the digital signal ds satisfies the rational number sampling rate required in the arbitrary standard to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the rational number decimation filter **150**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the mixer **130**, the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

FIGS. **10**A and **10**B are a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a ninth exemplary embodiments.

In FIGS. **10**A and **10**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIGS. **10**A and **10**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds to control the digital signal ds illustrated in FIG. **1** to be processed.

Here, referring to FIG. **10**A, in the input signal condition where the IQs are inconsistent and the digital signal ds does not satisfy an integer sampling rate required in the arbitrary standard, the signal processing controller **190** selects the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the IQ inconsistency compensating unit **170** and the IQ inconsistency compensating unit **170** transmits the digital signal ds in which a phase error of the In-phase signal and the quadrature signal is compensated in the digital signal ds to the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the IQ inconsistency compensating unit **170**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **10**B, in the input signal condition where the IQs are inconsistent and the digital signal ds does not satisfy an integer sampling rate required in the arbitrary standard, the signal processing controller **190** selects the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **10**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **10**A.

Differently from FIG. **10**A, in FIG. **10**B, the phase error of the In-phase signal and the quadrature signal is compensated in the IQ inconsistency compensating unit **170**, and the digital signal ds is integer-decimated in the integer decimation filter **140**, and then transmitted to the channel selecting filter **180**.

In FIGS. **10**A and **10**B, even though it is described that the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180**, but controls the digital signal ds to be automatically transmitted to the integer decimation filter **140**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with the set signal processing order. However, the invention is not limited thereto.

FIGS. **11**A and **11**B are a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a tenth exemplary embodiments.

In FIGS. **11**A and **11**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIGS. **11**A and **11**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **11**A, in the input signal condition where the IQs are inconsistent and the digital signal ds does not satisfy a rational number sampling rate required in the arbitrary standard, the signal processing controller **190** selects the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard, from the integer decimation filter **140**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the IQ inconsistency compensating unit **170** and the IQ inconsistency compensating unit **170** transmits the digital signal ds in which a phase error of the In-phase signal and the quadrature signal is compensated in the digital signal ds to the signal processing controller **190**.

Thereafter, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the IQ inconsistency compensating unit **170**, to the rational number decimation filter **150**.

The rational number decimation filter **150** performs the rational number decimation on the digital signal ds to transmit the rational number-decimated digital signal ds to the signal processing controller **190** and the signal processing controller **190** transmits the digital signal ds transmitted from the rational number decimation filter **150** to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **11**B, in the input signal condition where the IQs are inconsistent and the digital signal ds does not satisfy a rational number sampling rate required in the arbitrary standard, the signal processing controller **190** selects the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **11**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **11**A.

Differently from FIG. **11**A, in FIG. **11**B, the phase error of the In-phase signal and the quadrature signal is compensated in the IQ inconsistency compensating unit **170**, and the digital signal ds is integer-decimated in the integer decimation filter **140**, rational number-decimated in the rational number decimation filter **150**, and then transmitted to the channel selecting filter **180**.

In FIGS. **11**A and **11**B, even though it is described that the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180**, but controls the digital signal ds to be automatically transmitted to the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with the set signal processing order. However, the invention is not limited thereto.

FIGS. **12**A and **12**B are a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a ninth exemplary embodiments.

In FIGS. **12**A and **12**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIGS. **12**A and **12**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **12**A, in the input signal condition where the digital signal ds includes a DC component, the IQs are inconsistent, and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the DC offset compensating unit **160** and receives a digital signal ds in which the DC component is removed from the DC offset compensating unit **160**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the DC offset compensating unit **160**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard, from the integer decimation filter **140**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the IQ inconsistency compensating unit **170** and the IQ inconsistency compensating unit **170** transmits the digital signal ds in which a phase error of the In-phase signal and the quadrature signal is compensated in the digital signal dsto the signal processing controller **190**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the IQ inconsistency compensating unit **170**, to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the integer decimation filter **140**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **12**B, in the input signal condition where the digital signal ds includes a DC component, the IQs are inconsistent, and an integer sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **12**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **12**A.

Differently from FIG. **12**A, in FIG. **12**B, the integer decimation is performed on a digital signal ds first in the integer decimation filter **140**, the DC component is removed in the DC offset compensating unit **160**, the phase error of the In-phase signal and the quadrature signal is compensated in the IQ inconsistency compensating unit **170**, and then the digital signal ds is transmitted to the channel selecting filter **180**.

In FIGS. **12**A and **12**B, even though it is described that the integer decimation filter **140**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the integer decimation filter **140**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180**, but controls the digital signal to be automatically transmitted to the integer decimation filter **140**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with the set signal processing order. However, the invention is not limited thereto.

FIGS. **13**A and **13**B are a control block diagram of a control configuration of the digital RF receiver illustrated in FIG. **1** which is reconfigured according to a twelfth exemplary embodiments.

In FIGS. **13**A and **13**B, detailed description of repeated configurations of the configurations illustrated in FIG. **1** will be omitted or the repeated configurations will be briefly described.

Referring to FIGS. **13**A and **13**B, the digital RF receiver may include the low noise amplifier **110**, the signal converting unit **120**, the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, the channel selecting filter **180**, and the signal processing controller **190**.

The signal processing controller **190** selects at least one of the mixer **130**, the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with an input signal condition of the digital signal ds illustrated in FIG. **1** to control the digital signal ds to be processed.

Here, referring to FIG. **13**A, in the input signal condition where the digital signal ds includes the DC component, the IQs are inconsistent but a rational number sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the signal converting unit **120**, to the DC offset compensating unit **160** and receives a

digital signal ds in which the DC component is removed from the DC offset compensating unit **160**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the DC offset compensating unit **160**, to the integer decimation filter **140** and receives an integer-decimated digital signal ds which satisfies the integer sampling rate required in an arbitrary standard from the integer decimation filter **140**.

The signal processing controller **190** transmits the digital signal ds, which is transmitted from the integer decimation filter **140**, to the IQ inconsistency compensating unit **170** and the IQ inconsistency compensating unit **170** transmits the digital signal ds in which a phase error of the In-phase signal and the quadrature signal is compensated in the digital signal ds to the signal processing controller **190**.

Further, the signal processing controller **190** transmits the digital signal ds, which is transmitted from the IQ inconsistency compensating unit **170**, to the rational number decimation filter **150**.

The rational number decimation filter **150** performs the rational number decimation on the digital signal ds to transmit the rational number-decimated digital signal to the signal processing controller **190** and the signal processing controller **190** transmits the digital signal ds transmitted from the rational number decimation filter **150** to the channel selecting filter **180**.

The channel selecting filter **180** outputs a digital signal ds obtained by removing an interference signal to other processing device.

Here, the interference signal may be a noise signal which is flew in the digital signal ds from at least one of the integer decimation filter **140**, the rational number decimation filter **150**, the IQ inconsistency compensating unit **170**, and the signal processing controller **190**.

Also, the interference signal may be an original noise signal included in the RF signal, but the invention is not limited thereto.

Here, referring to FIG. **13**B, in the input signal condition where the digital signal ds includes the DC component and the IQs are inconsistent but a rational number sampling rate required in the arbitrary standard is not satisfied, the signal processing controller **190** selects the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** to process the digital signal ds in accordance with a set signal processing order.

That is, FIG. **13**B illustrates a different signal processing order in the input signal condition which is the same as FIG. **13**A.

Differently from FIG. **13**A, in FIG. **13**B, the integer decimation is performed on a digital signal ds first in the integer decimation filter **140**, the DC component is removed in the DC offset compensating unit **160**, the phase error of the In-phase signal and the quadrature signal is compensated in the IQ inconsistency compensating unit **170**, the digital signal ds is rational-number decimated in the rational number decimation filter **150** and then is transmitted to the channel selecting filter **180**.

In FIGS. **13**A and **13**B, even though it is described that the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** receive the digital signal ds through the signal processing controller **190**, the signal processing controller **190** does not receive the digital signal ds output from at least one of the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180**, but controls the digital signal ds to be automatically transmitted to the integer decimation filter **140**, the rational number decimation filter **150**, the DC offset compensating unit **160**, the IQ inconsistency compensating unit **170**, and the channel selecting filter **180** in accordance with the set signal processing order. However, the invention is not limited thereto.

The control configuration of the digital RF receiver according to the exemplary embodiments illustrated in FIGS. **2** to **13** has an advantage in that the signal processing order is determined in accordance with the input signal condition of the RF signal or the digital signal among the control configuration of the digital RF receiver illustrated in FIG. **1** and the signal is processed to reduce power consumption and a signal processing time.

As described above, the exemplary embodiments have been described and illustrated in the drawings and the specification. The exemplary embodiments were chosen and described in order to explain certain principles of the invention and their practical application, to thereby enable others skilled in the art to make and utilize various exemplary embodiments of the present invention, as well as various alternatives and modifications thereof. As is evident from the foregoing description, certain aspects of the present invention are not limited by the particular details of the examples illustrated herein, and it is therefore contemplated that other modifications and applications, or equivalents thereof, will occur to those skilled in the art. Many changes, modifications, variations and other uses and applications of the present construction will, however, become apparent to those skilled in the art after considering the specification and the accompanying drawings. All such changes, modifications, variations and other uses and applications which do not depart from the spirit and scope of the invention are deemed to be covered by the invention which is limited only by the claims which follow.

What is claimed is:

1. A digital radio frequency receiver, comprising: a signal converting unit which converts an radio frequency signal received from an external device into a digital signal;

a plurality of functional modules which process the digital signal in accordance with predetermined orders when the digital signal is input; and

a signal processing controller which selects at least one of the plurality of functional modules to control the digital signal to be processed in consideration of whether an intermediate frequency signal component is included in the digital signal or a sampling rate related with sampling information of the digital signal.

2. The digital radio frequency receiver of claim **1**, wherein: the plurality of functional modules, includes

a direct current offset compensating unit which removes a direct current component included in the digital signal;

an inphase and quadrature inconsistency compensating unit which compensates a phase error of an In-phase signal and a quadrature signal of the digital signal;

a mixer which removes the intermediate frequency signal from the digital signal and separates a phase;

an integer decimation filter which performs integer decimation so as to satisfy an integer sampling rate required for sampling information of the digital signal;

a rational number decimation filter which performs rational decimation so as to satisfy a rational number sampling rate of the digital signal; and

a signal processing unit which includes a channel selecting filter which removes an interference signal from the digital signal.

3. The digital radio frequency receiver of claim **2**, wherein:

when the intermediate frequency signal component is included in the digital signal and the sampling rate of the digital signal does not satisfy a predetermined integer sampling rate, the signal processing controller selects the mixer, the integer decimation filter, and the channel selecting filter and outputs the digital signal to the mixer, the integer decimation filter, and the channel selecting filter in accordance with a predetermined order.

4. The digital radio frequency receiver of claim **2**, wherein:

when the intermediate frequency signal component is included in the digital signal and the sampling rate of the digital signal does not satisfy a predetermined rational number sampling rate, the signal processing controller selects the mixer, the integer decimation filter, the rational number decimation filter, and the channel selecting filter and outputs the digital signal to the mixer, the integer decimation filter, the rational number decimation filter, and the channel selecting filter in accordance with a predetermined order.

5. The digital radio frequency receiver of claim **2**, wherein:

when the intermediate frequency signal component and the direct current component are included in the digital signal and the sampling rate of the digital signal does not satisfy a predetermined integer sampling rate, the signal processing controller selects the direct current offset compensating unit, the mixer, the integer decimation filter, and the channel selecting filter and outputs the digital signal to the direct current offset compensating unit, the mixer, the integer decimation filter, and the channel selecting filter in accordance with a predetermined order.

6. The digital radio frequency receiver of claim **2**, wherein:

when the intermediate frequency signal component and the direct current component are included in the digital signal and the sampling rate of the digital signal does not satisfy a predetermined rational number sampling rate, the signal processing controller selects the direct current offset compensating unit, the mixer, the integer decimation filter, the rational number decimation filter, and the channel selecting filter and outputs the digital signal to the direct current offset compensating unit, the mixer, the integer decimation filter, the rational number decimation filter, and the channel selecting filter in accordance with a predetermined order.

7. The digital radio frequency receiver of claim **2**, wherein:

when the intermediate frequency signal component is included in the digital signal and the sampling rate of the digital signal does not satisfy a predetermined integer sampling rate, the signal processing controller selects the inphase and quadrature inconsistency compensating unit, the mixer, the integer decimation filter, and the channel selecting filter and outputs the digital signal to the inphase and quadrature inconsistency compensating unit, the mixer, the integer decimation filter, and the channel selecting filter in accordance with a predetermined order.

8. The digital radio frequency receiver of claim **2**, wherein:

when the intermediate frequency signal component is included in the digital signal, the inphases and quadratures are inconsistent, and the sampling rate of the digital signal does not satisfy a predetermined rational number sampling rate, the signal processing controller selects the inphase and quadrature inconsistency compensating unit, the mixer, the integer decimation filter, the rational number decimation filter, and the channel selecting filter and outputs the digital signal to the inphase and quadrature inconsistency compensating unit, the mixer, the integer decimation filter, the rational number decimation filter, and the channel selecting filter in accordance with a predetermined order.

9. The digital radio frequency receiver of claim **2**, wherein:

when the intermediate frequency signal component and the direct current component are included in the digital signal, the inphases and quadratures are inconsistent, and the sampling rate of the digital signal does not satisfy a predetermined integer sampling rate, the signal processing controller selects the direct current offset compensating unit, the inphase and quadrature inconsistency compensating unit, the mixer, the integer decimation filter, and the channel selecting filter and outputs the digital signal to the direct current offset compensating unit, the inphase and quadrature inconsistency compensating unit, the mixer, the integer decimation filter, and the channel selecting filter in accordance with a predetermined order.

10. The digital radio frequency receiver of claim **2**, wherein:

when the intermediate frequency signal component and the direct current component are included in the digital signal, the inphases and quadratures are inconsistent, and the sampling rate of the digital signal does not satisfy a predetermined rational number sampling rate, the signal processing controller selects the direct current offset compensating unit, the inphase and quadrature inconsistency compensating unit, the mixer, the integer decimation filter, the rational number decimation filter, and the channel selecting filter and outputs the digital signal to the direct current offset compensating unit, the inphase and quadrature inconsistency compensating unit, the mixer, the integer decimation filter, the rational number decimation filter, and the channel selecting filter in accordance with a predetermined order.

11. The digital radio frequency receiver of claim **2**, wherein:

when the inphases and quadratures of the digital signal are inconsistent and the sampling rate of the digital signal does not satisfy a predetermined integer sampling rate, the signal processing controller selects the integer decimation filter, the inphase and quadrature inconsistency compensating unit, and the channel selecting filter and outputs the digital signal to the integer decimation filter, the inphase and quadrature inconsistency compensating unit, and the channel selecting filter in accordance with a predetermined order.

12. The digital radio frequency receiver of claim **2**, wherein:

when the inphases and quadratures of the digital signal are inconsistent and the sampling rate of the digital signal does not satisfy a predetermined rational number sampling rate, the signal processing controller selects the integer decimation filter, the inphase and quadrature inconsistency compensating unit, the rational number decimation filter, and the channel selecting filter and outputs the digital signal to the integer decimation filter, the inphase and quadrature inconsistency compensating unit, the rational number decimation filter, and the channel selecting filter in accordance with a predetermined order.

13. The digital radio frequency receiver of claim **2**, wherein:

when the direct current component is included in the digital signal, the inphases and quadratures are inconsistent, and the sampling rate of the digital signal does not satisfy a predetermined integer sampling rate, the signal processing controller selects the direct current offset compensating unit, the integer decimation filter, the inphase and quadrature inconsistency compensating unit, and the channel selecting filter and outputs the digital signal to the direct current offset compensating unit, the integer decimation filter, the inphase and quadrature inconsistency compensating unit, and the channel selecting filter in accordance with a predetermined order.

14. The digital radio frequency receiver of claim **2**, wherein:

when the direct current component is included in the digital signal, the inphases and quadratures are inconsistent, and the sampling rate of the digital signal does not satisfy a predetermined rational number sampling rate, the signal processing controller selects the direct current offset compensating unit, the integer decimation filter, the inphase and quadrature inconsistency compensating unit, the rational number decimation filter, and the channel selecting filter and outputs the digital signal to the direct current offset compensating unit, the integer decimation filter, the inphase and quadrature inconsistency compensating unit, the rational number decimation filter, and the channel selecting filter in accordance with a predetermined order.

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